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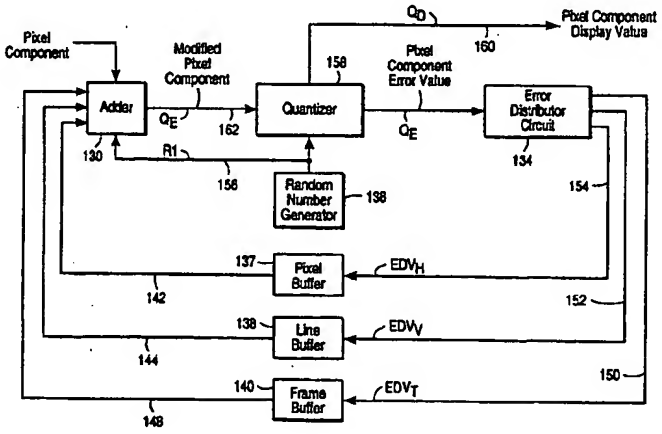

(57) Abstract

An image processor is provided for transforming true color pixels into display pixels with a reduced number of data bits. The image processor divides a pixel into its respective red, green, and blue components and applies multi–dimensional error diffusion to each component. The image processor applies a set of error diffusion values to a pixel component to obtain a modified pixel component. The error diffusion values include error diffusion values associated with pixels that are horizontally, vertically, and temporally displaced from a newly received pixel. Based on the modified pixel component, the image processor generates a pixel component display value and a pixel component error value. Each of the pixel component display values for a pixel are combined to form a display pixel, which is then forwarded to a display. The pixel component error value is distributed into temporal, vertical, and horizontal dimensional error diffusion values to be employed with later received pixels to generate modified pixel components. The pixel component error value can be divided among vertical, temporal, and horizontal dimensional error diffusion values in varying proportions. This non–fixed coefficient approach provides adaptability for different types of image sources.

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MULTI-DIMENSIONAL ERROR DIFFUSION WITH HORIZONTAL, VERTICAL AND TEMPORAL VALUES

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention is directed toward the field of image processing. More particularly, the present invention is directed toward multi-dimensional error diffusion.

Description of the Related Art

Many computer graphics and television images are generated as true color images, which are composed of pixels each represented by 24 bits of data. Each pixel includes a red pixel component, green pixel component, and blue pixel component. In a 24 bit true color pixel, each pixel component is typically represented by 8 bits of data. In many instances, it is necessary to transform true color images, so that each pixel is represented by less than 24 bits of data. For example, many flat panel liquid crystal displays ("LCD") are not capable of displaying pixels with colors spanning the approximate range of 16.7 million possible colors that can be represented by 24 data bits.

In order to provide for displaying true color images in an environment that cannot fully support true color images, such as a flat panel LCD, true color image pixels are transformed to be represented by a reduced number of data bits. For example, a 24 bit true color pixel may be transformed into a 16 bit display pixel in one environment. This is only one possible transformation. Many different transformations may be performed, depending upon the display environment being used. For instance, flat panel LCDs make use of display pixels represented by a variety of different data bit quantities, such as 3, 9, 12, and 18 data bits.

However, the transformation of a true color image's 24 bit true color pixels into display pixels with less than 24 bits results in a degradation of the image's color quality. Reducing the number of data bits in a pixel can severely limit the spectrum of available colors, in comparison to the approximately 16.7 million colors available to a 24 bit true color pixel. In order to compensate for such color degradation, a dithering technique can be employed to create a perception of 24 bit true color where only a limited color palette is actually available.

In one dithering technique, the most significant data bits from each pixel component in a true color pixel are employed as data bits for respective pixel

components in a display pixel. For each true color pixel component, a set of least significant bits, which have not been incorporated in a display pixel component, are used to generate a diffusion value. The diffusion value is then employed in the transformation of another true color pixel component as part of an error diffusion process.

The diffusion value is employed to diffuse the color of the true color pixel among neighboring display pixels, so that color degradation can be reduced. A diffusion value derived from a true color pixel can be employed in the generation of a neighboring display pixel that is:

- in the same image pixel row as the true color pixel (horizontal dithering);
- in the same image pixel column as the true color pixel (vertical dithering); or
- in a subsequent image at the same pixel coordinates as the true color pixel (temporal dithering).

Traditional systems have not provided for performing horizontal, vertical, and temporal dithering at the same time. Instead, traditional systems only perform 1 or 2 types of dithering.

Different types of images respond better to different dithering techniques. For example, television images are generally not enhanced significantly by dithering performed between pixels in different sequential images (temporal dithering), while computer graphics images benefit considerably from temporal dithering. This is because a television image lacks temporal correlation, and many computer graphics images have a high level of temporal correlation. Existing dithering systems are not equipped to optimally provide for the processing of both television and computer graphics images, since such systems typically provide a fixed level of dithering between pixels in different sequential images.

Accordingly, there is a need for an image processor that provides for performing vertical, horizontal, and temporal dithering at the same time. Further, it is desirable for the level of dithering among the vertical, horizontal, and temporal dimensions to be adjustable to best suit different types of images. It is also beneficial for such an image processor to provide for the transformation of true color image pixels into display pixels with a reduced number of data bits, where the reduced number of data bits is variable.

SUMMARY OF THE INVENTION

An image processor is provided for transforming true color pixels into display pixels with a reduced number of data bits. In performing such a transformation, the image processor divides a pixel into its respective red, green, and blue components and applies multi-dimensional error diffusion to each component. For each received pixel component, the image processor applies a set of error diffusion values to obtain a modified pixel component. The error diffusion values include error diffusion values associated with pixels that are horizontally, vertically, and temporally displaced from the received pixel. As a result, the image processor supports the application of vertical, horizontal, and temporal dithering at the same time.

Based on the modified pixel component, the image processor generates a pixel component display value and a pixel component error value. Each of the pixel component display values for a pixel are combined to form a display pixel, which is then forwarded to a display. After deriving the component display value from the modified pixel component, a component error value is generated. The component error value is then distributed into temporal, vertical, and horizontal dimensional error diffusion values to be employed with later received pixels to generate modified pixel components.

In distributing the pixel component error values, different portions of the pixel component error value can be divided among vertical, temporal, and horizontal dimensional error diffusion values. These portions are adjustable. This enables different types of dimensional error diffusion values to be either increased or decreased in importance, based on the types of images that are being processed. For example, television images are not very responsive to temporal dimensional error diffusion values while computer graphics images respond quite well to temporal dimensional error diffusion values.

These and other objects and advantages of the present invention will appear more clearly from the following description in which the preferred embodiment of the invention has been set forth in conjunction with the drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention will be described with reference to the following drawings, in which:

Fig. 1 illustrates an image processing system including an image processor in accordance with the present invention.

Fig. 2 illustrates a sequence of operations performed by an image processor

in accordance with the present invention.

Fig. 3 illustrates an image processor in accordance with the present invention.

Fig. 4 illustrates a sequence of operations for applying dimensional error diffusion values to a pixel in accordance with the present invention.

Fig. 5 illustrates a block diagram of a quantizer in the image processor shown in Fig. 3, in one embodiment of the present invention.

Fig. 6 illustrates a sequence of operations for distributing a pixel component error value in accordance with the present invention.

Fig. 7 illustrates an error distributor circuit employed in one embodiment of the present invention.

Fig. 8 illustrates a sequence of operations for determining a temporal dimensional error diffusion value in one of embodiment of the present invention.

Fig. 9 illustrates a block diagram of the temporal error circuit shown in Fig. 7 in one embodiment of the present invention.

Figs. 10(a)-(c) illustrate circuitry employed in the temporal error circuit shown in Fig. 9 in one embodiment of the present invention.

Fig. 11 illustrates a sequence of operations for determining a vertical dimensional error value in one embodiment of the present invention.

Fig. 12 illustrates a block diagram of the vertical error circuit shown in Fig. 7 in one embodiment of the present invention.

Figs. 13(a)-(c) illustrate circuitry employed in the vertical error circuit shown in Fig. 12 in one embodiment of the present invention.

Fig. 14 illustrates a block diagram of the horizontal error circuit shown in Fig. 7 in one embodiment of the present invention.

Fig. 15 illustrates circuitry employed in the mask circuit of the horizontal error circuit shown in Fig. 14 in one embodiment of the present invention.

DETAILED DESCRIPTION

In accordance with the present invention, an image processor is provided for transforming pixels in an image. In one embodiment of the present invention, a 24 bit true color pixel is transformed into a display pixel having one of a selectable number of data bits. In one such embodiment, the 24 bit true color pixel can be transformed into either a 3, 9, 12, 18, or 24 bit display pixel. As part of the transformation, error diffusion values are applied to pixel components to simultaneously achieve vertical, horizontal, and temporal dithering. Pixel component

error values from vertically, horizontally, and temporally displaced pixels are employed. When establishing error diffusion values for pixels in different types of images, such as computer graphics and television images, different levels of significance are given to the vertical, horizontal, and temporal dithering.

An image processor in accordance with the present invention also adds perturbations when determining error diffusion values. Perturbations provide for the removal of artifacts that can result in a display image when dithering is employed. The image processor provides for varying the perturbations, so there is an increased level of randomness which aids in the removal of artifacts.

Fig. 1 illustrates system 100, which includes image processor 101 for transforming pixels in accordance with the present invention. Image processor 101 has an input coupled to receive pixels from image source 103 and an output coupled to provide transformed display pixels to display 102. Image processor 101 includes red pixel component image processor 104, green pixel component image processor 105, and blue pixel component image processor 106. Upon receiving a pixel, image processor 101 divides the pixel into its respective red, green, and blue components and provides each component to a corresponding one of pixel component image processors 104, 105, and 106.

Each pixel component image processor 104, 105, 106 applies a set of dimensional error diffusion values to an incoming pixel component and generates a pixel component display value. The pixel component display values from pixel component image processors 104, 105, and 106 are combined to form the transformed display pixel value at the output of image processor 101. In one embodiment, such a combination is achieved by concatenating the outputs of pixel component image processors 104, 105, and 106.

Fig. 2 illustrates a sequence of operations performed by each pixel component image processor 104, 105, 106 in image processor 101 in one embodiment of the present invention. First, a pixel component is received in step 110. Next, a set of dimensional error diffusion values are added to the pixel component to obtain a modified pixel component ("MPC") in step 112. In one embodiment of the present invention, the set of dimensional error diffusion values includes temporal, vertical, and horizontal dimensional error diffusion values. In yet another embodiment, the set of dimensional error diffusion values includes a random number.

A pixel component display value and pixel component error value are generated in step 114. The pixel component error value is employed to generate error

diffusion values to be used in future pixel transformations. As part of step 114, the pixel component display value is generated in step 116, and the pixel component error value is generated in step 118.

In one embodiment of the present invention, the pixel component display value is generated in step 116 by selecting the most significant bits in the modified pixel component obtained in step 112. In such an embodiment, the pixel component image processor first determines the number of bits to be employed in the resulting display pixel. This value can be provided by a system user or another alternate source. Next, the number of most significant bits to be selected is set to equal one-third of the number of bits in the display pixel to be provided on the output of image processor 101. Finally, the desired number of most significant bits in the modified pixel component value are selected to be the pixel component display value. For example, if image processor 101 is to provide a display pixel with 9 data bits, then a pixel component display value is obtained by selecting the 3 most significant bits of the modified pixel component. In an alternate embodiment of the present invention, different display pixel bit lengths are employed, such as 3, 12, 18, and 24.

In one embodiment of the present invention, the modified pixel component is clamped to a value in a predetermined range, prior to the bits for the pixel component display value being selected. In one such embodiment, the modified pixel component is clamped to be a value ranging from 0 to 255. The pixel component display value is then selected from the clamped modified pixel component.

In order to generate the pixel component error value in step 118, in one embodiment of the present invention, a set of values are subtracted from the modified pixel component. This set of values includes the pixel component display value generated in step 116. In further embodiments of the present invention, the set of values being subtracted includes the pixel component display value and at least one of the dimensional error diffusion values added to the incoming pixel component in step 112. In one embodiment, a random number is added to an incoming pixel component in step 112 as a dimensional error diffusion value to add perturbation. This random number is then subtracted from the modified pixel component in step 118, along with the pixel component display value, in order to obtain the pixel component error value.

Once the pixel component display value and pixel component error value are obtained in step 114, the distribution of the pixel component error value is performed in step 120. The distribution provides for the generation of a vertical dimensional

error diffusion value ("EDVV "), temporal dimensional error diffusion value ("EDVT"), and horizontal dimensional error diffusion value ("EDVH"). The EDVV, EDVT, and EDVH will be added to later received pixel components as part of generating a modified pixel component (step 112).

The EDVV is to be applied to a pixel component of a later received pixel in the same image and column of pixels as the pixel from which the EDVV has been derived (vertical dithering). The EDVT is to be applied to a pixel component of a later received pixel in an image that follows the image containing the pixel from which the EDVT has been derived (temporal dithering). In one embodiment of the present invention, the later received pixel has the same image location (row and column) as the pixel from which the EDVT was derived. The EDVH is to be applied to a later received pixel component of a pixel in the same image and row of pixels as the pixel from which the EDVH has been derived (horizontal dithering). Once the pixel component error value has been distributed, the process shown in Fig. 2 is done. By performing a distribution (step 120) of EDVV, EDVT, and EDVH, three dimensional error diffusion is achieved to provide for vertical, temporal, and horizontal dithering.

Fig. 3 depicts circuitry for use in each of the pixel component image processors 104, 105, and 106 for performing the sequence of operations illustrated in Fig. 2, in one embodiment of the present invention. The pixel component image processor circuitry shown in Fig. 3 includes adder 130 having a set of inputs coupled to receive the following:

- Pixel component ("PC");
- Random number R1 from random number generator 136;
- EDVH from pixel buffer 137;
- EDVV from line buffer 138; and
- EDVT from frame buffer 140.

EDVH, EDVV, EDVT, and R1 constitute a set of dimensional error diffusion values, which are added to the pixel component (PC) by adder 130 to obtain a modified pixel component (Fig. 2, step 112).

Output 162 of adder 130 is coupled to quantizer 132 to provide the modified pixel component. Quantizer 132 is also coupled to random number generator 136 to receive random number R1. Quantizer 132 provides a pixel component display value QD on output 160 and a pixel component error value QE on output 158. In order to generate pixel component display value QD (Fig. 2, step 116), quantizer 132 selects a set of most significant bits in the modified pixel component. The number of most

significant bits selected is equal to one-third of the number of bits in the display pixel provided at the output of image processor 101 (Fig. 1).

In one embodiment of the present invention, quantizer 132 generates the pixel component error value QE (Fig. 2, step 118) according to the following equation:

QE = MPC - QDN - R1

wherein:

QDN is a normalized version of the pixel component display value QD.

In one embodiment of the present invention, QD has less bits than R1 and MPC, which have the same number of bits. In such an embodiment, QD is normalized to form QDN, which can be used to subtract the pixel component display value from the modified pixel component. The normalization of QD results in the number of bits in QDN being the same as the number of bits in MPC and R1. If QD already has the same number of bits as MPC and R1, then QDN is equal to QD.

In one embodiment, R1 has 13 bits; MPC has 13 bits; and QD has 3 bits. In such an embodiment, QD is normalized to form QDN, which has 13 bits. The normalization is achieved by repeating the bit pattern of QD, until the number of bits in QDN is greater than or equal to the number of bits in MPC. The QDN is then truncated by removing the least significant bits, until QDN has the same number of bits as MPC. In the above example, QD has the 3 bit pattern 010. After normalization, the 13 bit pattern for QDN is 0100100100100.

Quantizer output 158 is coupled to error distributor 134 to provide the pixel component error value QE. Error distributor 134 processes the pixel component error value to obtain horizontal dimensional error diffusion value EDVH, vertical dimensional diffusion value EDVV, and temporal dimensional error diffusion value EDVT. EDVH is provided on error distributor output 154, which is coupled to the input of pixel buffer 137. EDVV is provided on error distributor output 152, which is coupled to the input of line buffer 138. EDVT is provided on error distributor output 150, which is coupled to the input of frame buffer 140.

Pixel buffer output 142 is coupled to adder 130 for providing horizontal dimensional error diffusion values. Line buffer output 144 is coupled to adder 130 for providing vertical dimensional error diffusion values, and frame buffer output 148 is coupled to adder 130 for providing temporal dimensional error diffusion values.

Fig. 4 illustrates a sequence of operations performed in one embodiment of the present invention to provide for the addition of dimensional error diffusion values to a pixel component to create a modified pixel component (Fig. 2, step 112). The

sequence of operations shown in Fig. 4 illustrates how adder 130, pixel buffer 137, line buffer 138, frame buffer 140, and random number generator 136 operate in conjunction with one another to provide the modified pixel component at adder output 162.

A determination is made in step 170 of whether the pixel component most recently received by adder 130 is the first pixel in an image's row of pixels. If the most recently received pixel is the first pixel in a row, then a zero value EDVH is provided to adder 130 by pixel buffer 137 (step 172). Otherwise, pixel buffer 137 provides adder 130 with an EDVH equal to the EDVH value determined by error distributor 134 for the immediately preceding pixel received by adder 130 (step 174).

Once an EDVH value has been provided to adder 130, it is determined whether the most recently received pixel component is from a pixel in an image's first row (step 176). If the pixel component is determined to be from a pixel in an image's first row, then line buffer 138 provides adder 130 with a zero value EDVV (step 178). Otherwise, line buffer 138 provides adder 130 with an EDVV value equal to the EDVV value determined by error distributor 134 for the pixel in the image's immediately proceeding pixel row in the same column of pixels as the most recently received pixel (step 180).

Once an EDVV value has been provided, a determination is made in step 182 of whether the pixel component received by adder 130 is from a pixel in a first image in a set of images. If it is determined that the pixel component is from a pixel in a first image, then frame buffer 140 provides adder 130 with a zero value EDVT (step 184). Otherwise, frame buffer 140 provides adder 130 with an EDVT value calculated by error distributor 134 for a pixel in an image that immediately precedes the present image and has the same row and column locations as the most recently received pixel (step 186).

After an EDVT value is provided, a modified pixel component is calculated in step 188. In one embodiment of the present invention, the modified pixel component is calculated by adding the pixel component (PC) received by adder 130 to the EDVH, EDVV, EDVT, and a R1 error diffusion values provided to adder 130.

The above described process for generating a modified pixel component provides for three-dimensional error diffusion and perturbation. The resulting modified pixel component has received error diffusion and perturbation from the following:

- A temporally displaced pixel, which is in the same row and column as the most recently received pixel, in the immediately preceding image

(EDVT providing temporal dimensional error diffusion);

- A vertically displaced pixel, which is in the same image and column as the most recently received pixel, in the immediately preceding row of pixels (EDVV providing vertical dimensional error diffusion);
- A horizontally displaced pixel, which is in the same image and row as the most recently received pixel, in the immediately preceding column of pixels (EDVH providing horizontal dimensional error diffusion); and
- A random number (R1 providing perturbation).

By providing error diffusion from three dimensions, the amount of color degradation resulting from a reduced number of bits in the pixel component display value (QD) is lessened. Further, the addition of a random number to the pixel component aids in breaking up undesirable artifacts that can be induced by error diffusion. As a result, the modified pixel component can be employed to generate a pixel component display value QD, that better provides a perception of true color than pixel components derived by traditional image processing systems without three dimensional error diffusion.

In alternate embodiments of the present invention, the order of the above described process steps (Fig. 4) can be altered so that the EDVH , EDVV , and EDVT values are either provided to adder 130 in a different order or simultaneously. In yet another embodiment of the present invention, no R1 value is employed in the calculation of MPC (step 188).

Fig. 5 illustrates a block diagram of quantizer 132 in one embodiment of the present invention. As described above, quantizer 132 is coupled to output 162 of adder 130 to receive the modified pixel component. Quantizer 132 includes clamp circuit 163 having an input coupled to receive the modified pixel component and an output coupled to shifter 164. Clamp circuit 163 clamps the value of the modified pixel component to be between 0 and 255, and provides the clamped value on its output. Shifter 164 also receives a primary bits value. The primary bits value identifies the number of bits to be included in the pixel component display value (QD) provided on quantizer output 160. The output of shifter 164 forms quantizer output 160 to provide a set of most significant bits from the clamped modified pixel component as the pixel component display value (QD). The number of most significant bits that are provided by shifter 164 is designated by the primary bits value.

The output of shifter 164 is also provided to the input of scaler 165. Scaler

165 generates a normalized pixel component display value and is coupled to provide the normalized pixel component display value to an input of subtractor 166. Subtractor 166 has another input coupled to receive the modified pixel component. Subtractor 166 subtracts the pixel component display value from the modified pixel component and provides a resulting difference on an output coupled to an input of subtractor 167. Subtractor 167 has another input coupled to receive random number R1 from random number generator 136. Subtractor 167 subtracts random number R1 from the difference provided by subtractor 166. The resulting difference from subtractor 167 is provided on quantizer output 158 as the pixel component error value (QE).

Fig. 6 illustrates a sequence of operations performed by error distributor 134 (Fig. 3) for distributing the quantizer error QE (Fig. 2, step 120) provided on output 158 of quantizer 132 (Fig. 3). A temporal dimensional error diffusion value is determined in step 190. A vertical dimensional error diffusion value is determined step 192, and a horizontal dimensional error diffusion value is determined in step 194. Although Fig. 6 shows EDVT , EDVV and EDVH being determined sequentially, in alternate embodiments of the present invention, these values are determined simultaneously. In further embodiments, the values shown in Fig. 6 are determined sequentially, but in a different order than that shown in Fig. 6.

Fig. 7 illustrates a block diagram of error distributor 134 (Fig. 3) in one embodiment of the present invention. The error distributor 134 includes a temporal error circuit 204, vertical error circuit 212, and horizontal error circuit 216 that work together to distribute the pixel component error value QE into temporal (EDVT), vertical (EDVV), and horizontal (EDVH) components. In accordance with the present invention, QE can be distributed in a variety of selectable allocations, so that more or less emphasis can be placed on the temporal, vertical, and horizontal components. For example, when operating a computer graphics environment, more of QE can be distributed to temporal component EDVT than to EDVH and EDVV.

As shown in Fig. 7, error distributor 134 includes random number generator 200 having an output coupled to provide random number R2 to temporal error circuit 204. Temporal error circuit 204 is also coupled to receive the pixel component error value QE and the following signals:

- T-SHIFT — a weighting value employed for setting the allocation of QE to the generation of EDVT;
- T-BITS — a value identifying a number of bits extracted from

QE to represent a temporal error component; and

- T-PERTURB — a signal employed for adding randomness to the generation of a temporal dimensional error diffusion value.

Temporal error circuit 204 employs its inputs to produce an expanded temporal dimensional error diffusion value (TERR) on output 205, which is coupled to the input of shifter 206. Shifter 206 is also coupled to receive the T-SHIFT and T-BITS signals for determining the bits to be selected from the expanded temporal dimensional error diffusion value (TERR) to form EDVT. Based on the value of T-BITS, shifter 206 selects between zero and 3 of the bits in TERR to create the temporal dimensional error diffusion value (EDVT) that is supplied to frame buffer 140.

The expanded temporal dimensional error diffusion value (TERR) is reduced in size to create the temporal dimensional error diffusion value (EDVT), in order to conserve memory space in frame buffer 140. When EDVT is later provided to adder 130 (Fig. 3), zero value bits are appended to EDVT as least significant bits, so that EDVT has the same number of bits as the pixel component (PC) to which EDVT is being added.

Error distributor 134 also includes random number generator 208 having an output coupled to provide random number R3 to vertical error circuit 212. Vertical error circuit 212 is also coupled to receive the pixel component error value QE and the following signals:

- V-SHIFT — a weighting value employed for setting the allocation of QE to the generation of EDVV;
- V-BITS — a value identifying a number of bits extracted from QE to represent a vertical error component; and
- V-PERTURB — a signal employed for adding randomness to the generation of a vertical dimensional error diffusion value.

Vertical error circuit 212 employs its inputs to produce an expanded vertical dimensional error diffusion value (VERR) on output 213, which is coupled to the input of shifter 214. Shifter 214 also is coupled to receive the V-SHIFT and V-BITS signals for determining the bits to be selected from the expanded vertical dimensional error diffusion value (VERR) to form EDVV. Based on the value of V-BITS, shifter 214 selects between zero and 3 of the bits in VERR to create the vertical dimensional error

diffusion value (EDVV) that is supplied to line buffer 138.

The expanded vertical dimensional error diffusion value (VERR) is reduced in size to create the vertical dimensional error diffusion value (EDVV), in order to conserve memory space in line buffer 138. When EDVV is later provided to adder 130 (Fig. 3), zero value bits are appended to EDVV as least significant bits, so that EDVV has the same number of bits as the pixel component (PC) to which EDVV is being added.

Finally, horizontal error circuit 216 is included in error distributor 134 for generating a horizontal error diffusion value (EDVH) on output 217. Horizontal error circuit 216 receives and employs the same signals as temporal error circuit 204 and vertical error circuit 212 to generate EDVH. In one embodiment of the present invention, EDVH is allocated the portion of QE that is not allocated to EDVT and EDVV. This is achieved in one embodiment by subtracting the sum of TERR and VERR from QE.

Fig.8 illustrates a sequence of operations performed by temporal error circuit 204 in determining an expanded temporal dimensional error diffusion value (TERR). A temporal bit mask (TMASK) is generated in step 220, based on the T-SHIFT and T-BITS inputs. The temporal bit mask identifies the bits in QE, if any, that will be employed in establishing TERR.

Next, in step 222, a temporal perturbation factor (PFT) is generated, based on the R2 and T-PERTURB inputs. Perturbation factor PFT is used for adding randomness in the generation of a temporal dimensional error diffusion value. As described above, the addition of randomness aids in breaking up unpleasant artifacts that can be formed by the error diffusion process. Once the temporal bit mask and perturbation factor are generated, a mask operation is applied in step 224. The mask operation (224) uses TMASK and PFT, along with QE and T-BITS, to generate the expanded temporal dimensional error diffusion value (TERR).

Fig. 9 shows a block diagram of temporal error circuit 204 in one embodiment of the invention for carrying out the process steps described in Fig. 8. As shown in Fig. 9, temporal error circuit 204 includes perturbation factor circuit 230, bit mask circuit 234, and mask circuit 232. Perturbation factor circuit 230 receives the R2 random number and T-PERTURB signals, which are employed to generate a temporal perturbation factor (PFT) on output 236. Bit mask circuit 234 receives the T-SHIFT and T-BITS signals, which are employed to generate a temporal bit mask (TMASK) on output 237. Mask circuit 232 is coupled to receive perturbation factor PFT,

temporal bit mask TMASK, T-BITS, and pixel component error value QE. The mask circuit 232 combines these inputs to form the expanded temporal dimensional error diffusion value (TERR).

Fig. 10(a) illustrates circuitry employed in one embodiment of the present invention to form perturbation factor circuit 230. A 13 bit R2 input is coupled to third (D2) and fourth (D3) data inputs of multiplexer 241. Select bit zero (S0) of multiplexer 241 is coupled to the least significant bit of the T-PERTURB input, and select bit one (S1) is coupled to the most significant bit of the T-PERTURB input. A first data input (D0) of multiplexer 241 is set to hexadecimal value 1FFF, and a second data input (D1) of multiplexer 241 is coupled to the output of multiplexer 240. The select input of multiplexer 240 is coupled to the least significant bit of the R2 input. A first data input (D0) of multiplexer 240 is coupled to hexadecimal value 0000, and a second data input (D1) of multiplexer 240 is coupled to hexadecimal value 1FFF.

The output of multiplexer 241 provides a 13 bit temporal perturbation factor (PFT) output for perturbation factor circuit 230.

Fig. 10(b) illustrates circuitry employed in bit mask circuit 234 in one embodiment of the present invention. Multiplexer 243 operates to select a mask bit pattern. Multiplexer 243 has a first data input (D0) coupled to receive hexadecimal value 0000. Second (D1) and third (D2) data inputs of multiplexer 243 are coupled to receive hexadecimal value 0080. A fourth data input (D3) of multiplexer 243 is coupled to receive hexadecimal value 00C0. A first select input (S0) of multiplexer 243 is coupled to receive the least significant bit of the T-BITS input, and a second select input (S1) of multiplexer 243 is coupled to receive the most significant bit of the T-BITS inputs. An output of multiplexer 243 is coupled to an input of shifter 244 to provide a mask bit pattern.

Shifter 244 sets bit locations for the mask bit pattern provided by multiplexer 243. Shifter 244 is coupled to receive the T-BITS input and the T-SHIFT input. In operation, shifter 244 provides a 13 bit TMASK value according to the following rules:

- If T-BITS equals 3, then the input to shifter 244 is shifted right by (6 -T-SHIFT); else
- The input to shifter 244 is shifted right by (7 - T-SHIFT).

The resulting TMASK value has ones in the data bit locations that correspond to the bits in pixel component error value QE that are to be used in generating TERR.

The T-BITS input serves the purpose of identifying how many QE bits are used, and the T-SHIFT input identifies which QE bits to use and the amount of weight to be given to the TERR value. The weight is set by establishing which bit locations in TMASK will contain ones identifying bits from QE.

Fig. 10(c) illustrates circuitry to be employed in mask circuit 232. The most significant bit of 13 bit input QE is coupled to the input of sign extender 245, which provides an output with all bit values set to the same value as the most significant bit of QE. When QE is a signed value, the use of the most significant QE bit enables the sign to be utilized in determining TERR. And gate 242 has a first input coupled to receive TMASK and a second input coupled to receive PFT. The output of And gate 242 provides a masked temporal perturbation factor (PFTM), which is coupled to a third (D2) and fourth (D3) data input of multiplexer 249.

First (D0) and second (D1) data inputs of multiplexer 249 are coupled to hexadecimal value 0000. A first select input (S0) of multiplexer 249 is coupled to the least significant bit of the T-BITS input, and a second select input (S1) of multiplexer 249 is coupled to the most significant bit of the T-BITS input. In operation, the output of multiplexer 249 is set to zero when the T-BITS value is either zero or 1. The output of multiplexer 249 is set to the PFTM value provided at the output of And gate 242, when the T-BITS value is set to either 2 or 3.

The output of sign extender 245 is coupled to the input of inverter 247, which has an output coupled to a first input of And gate 248. The second input of And gate 248 is coupled to the output of And gate 242, which provides PFTM. The output of And gate 248 is coupled to a first data input (D0) of multiplexer 250, and the output of multiplexer 249 is coupled to a second data input (D1) of multiplexer 250. A select input of multiplexer 250 is coupled to the most significant bit of QE. In operation, multiplexer 250 provides the PFTM value from the output of And gate 242, when the most significant bit of QE is equal to zero. When the most significant bit of QE is equal to 1, the output of multiplexer 250 is set as follows:

- The PFTM value provided at the output of And gate 242, when the T-BITS value equals 2 or 3; else
- Zero, when the T-BITS value equals 0 or 1.

Pixel component error value QE is coupled to a first input of And gate 251, and the output of multiplexer 250 is coupled to a second input of And gate 251. The output of And gate 251 is coupled to a first input of Or gate 255.

The PFTM output of And gate 242 is also coupled to the input of inverter

246, which has an output coupled to the first input of And gate 252. A second input of And gate 252 is coupled to the TMASK value. The output of And gate 252 is coupled to a first input of Or gate 253, which has a second input coupled to the output of sign extender 245.

Multiplexer 254 has a select input coupled to the most significant bit of QE. A first data input (D0) of multiplexer 254 is coupled to hexadecimal value 0000, and a second data input (D1) of multiplexer 254 is coupled to the output of Or gate 253. In operation, the output of multiplexer 254 provides hexadecimal value 0000, when the most significant bit of QE is zero. If the most significant bit of QE is 1, then the output of multiplexer 254 is equal to hexadecimal value 1FFF. The output of multiplexer 254 is coupled to the second data input of Or gate 255, which provides the TERR value.

In operation, mask circuit 232 operates to provide the following TERR values:

- When the most significant bit of QE is 1, then the TERR value is equal to hexadecimal value 1FFF; and
- When the most significant bit of QE is equal to zero, then the TERR value is equal to the PFTM output of And gate 242 Anded with QE.

Returning to Fig. 7, it is seen that the temporal error circuit output TERR is coupled to the input of shifter 206. The 8 least significant bits of TERR are provided to shifter 206. Shifter 206 employs the T-BITS and T-SHIFT signals to convert TERR into EDVT. The T-BITS signal identifies whether EDVT will have a sign bit. If T-BITS is equal to zero, EDVT will be equal to zero. If T-BITS is equal to 1, then EDVT will not contain a sign bit. In this instance, the TERR bit corresponding to the T-SHIFT value is loaded as the EDVT value and padded by 2 leading zeroes. For example, if T-SHIFT is equal to 3, then bit [3] of the TERR value provided to the input of shifter 206 is padded by 2 leading zeroes and used as EDVT.

When T-BITS is equal to 2 or 3, the EDVT value includes a sign bit as the most significant bit. In this instance, shifter 206 sets the most significant bit of EDVT equal to the most significant bit of QE. For T-BITS equal to 2, the least significant bit of EDVT is set to equal the TERR bit corresponding to the T-SHIFT value. The next least significant EDVT bit is also equal to the most significant bit of QE to provide for sign extension.

For T-BITS equal to 3, the least significant bit of EDVT is equal to the TERR bit corresponding to the T-SHIFT value, and the next least significant EDVT bit is equal to the [T-SHIFT +1] bit of the TERR value. For example, if T-SHIFT is equal

to 3, and T-BITS is equal to 3, then bit [3] of the TERR value provided to the input of shifter 206 is selected to fill the least significant bit of EDVT. The next least significant bit of EDVT is set equal to bit [4] of TERR. The following EDVT bit is the most significant bit and is set to the most significant bit of QE.

Fig. 11 illustrates a sequence of operations performed by vertical error circuit 212 (Fig. 7) in determining an expanded vertical dimensional error diffusion value (VERR). A vertical bit mask (VMASK) is generated in step 280, based on the V-SHIFT and V-BITS inputs. The vertical bit mask identifies the bits in QE, if any, that will be employed in establishing VERR.

Next, in step 282, a vertical perturbation factor (PFV) is generated, based on the R3 and V-PERTURB inputs. Perturbation factor PFV is used for adding randomness in the generation of a vertical dimensional error diffusion value. As described above, the addition of randomness aids in breaking up unpleasant artifacts that can be formed by the error diffusion process. Once the vertical bit mask and perturbation factor are generated, a mask operation is applied in step 284. The mask operation (284) uses VMASK and PFV, along with QE and V-BITS, to generate the expanded vertical dimensional error diffusion value (VERR).

Fig. 12 shows a block diagram of vertical error circuit 212 in one embodiment of the invention for carrying out the process steps described in Fig. 11. As shown in Fig. 12, vertical error circuit 212 includes perturbation factor circuit 290, bit mask circuit 294, and mask circuit 292. Perturbation factor circuit 290 receives the R3 random number and the V-PERTURB signals, which are employed to generate a vertical perturbation factor (PFV) on output 296. Bit mask circuit 294 receives the V-SHIFT and V-BITS signals, which are employed to generate a vertical bit mask (VMASK) on output 297. Mask circuit 292 is coupled to receive perturbation factor PFV, vertical bit mask VMASK, V-BITS, and pixel component error value QE. The mask circuit 292 combines these inputs to form the expanded vertical dimensional error diffusion value (VERR).

Fig. 13(a) illustrates circuitry employed in one embodiment of the present invention to form perturbation factors circuit 290. A 13 bit R3 input is coupled to third (D2) and fourth (D3) data inputs of multiplexer 301. Select bit zero (S0) of multiplexer 301 is coupled to the least significant bit of the V-PERTURB input, and select bit on (S1) is coupled to the most significant bit of the V-PERTURB input. A first data input (D0) of multiplexer 301 is set to hexadecimal value 1FFF, and a second data input (D1) of multiplexer 301 is coupled to the output of multiplexer 300.

The select input of multiplexer 300 is coupled to the least significant bit of the R3 input. A first data input (D0) of multiplexer 300 is coupled to hexadecimal value 0000, and a second data input (D1) of multiplexer 300 is coupled to hexadecimal value 1FFF.

The output of multiplexer 301 provides a 13 bit vertical perturbation factor (PFV) output for perturbation factor circuit 290.

Fig. 13(b) illustrates circuitry employed in bit mask circuit 294 in one embodiment of the present invention. Multiplexer 303 selects a mask bit pattern. Multiplexer 303 has a first data input (D0) coupled to receive hexadecimal value 0000. Second (D1) and third (D2) data inputs of multiplexer 303 are coupled to receive hexadecimal value 0080. A fourth data (D3) input of multiplexer 303 is coupled to receive hexadecimal value 00C0. A first select input (S0) of multiplexer 303 is coupled to receive the least significant bit of the V-BITS input, and a second select input (S1) of multiplexer 303 is coupled to receive the most significant bit of the V-BITS input. An output of multiplexer 303 is coupled to an input of shifter 304 to provide a mask bit pattern.

Shifter 304 sets bit locations for the mask bit pattern provided by multiplexer 303. Shifter 304 is coupled to receive the V-BITS input and the V-SHIFT input. In operation, shifter 304 provides a 13 bit VMASK value according to the following rules:

- If V-BITS equals 3, then the input to shifter 304 is shifted right by (6 - V-SHIFT); else
- The input to shifter 304 is shifted right by (7 - V-SHIFT).

The resulting VMASK value has ones in the data bit locations that correspond to the bits in pixel component error value QE that are to be used in generating VERR. The V-BITS input serves the purpose of identifying how many QE bits are used, and the V-SHIFT input identifies which QE bits to use and the amount of weight to be given to the VERR value. The weight is set by establishing which bit locations in VMASK will contain ones identifying bits from QE.

Fig. 13(c) illustrates circuitry employed in mask circuit 292 in one embodiment of the invention. The most significant bit of 13 bit input QE is coupled to the input of sign extender 305, which provides an output with all bit values set to the same value as the most significant bit of QE. And gate 302 has a first input coupled to receive VMASK and a second input coupled to receive PFV. The output of And gate 302 provides a masked vertical perturbation factor (PFVM), which is

coupled to third (D2) and fourth (D3) data input of multiplexer 309.

First (D0) and second (D1) data inputs of multiplexer 309 are coupled to hexadecimal value 0000. A first select input (S0) of multiplexer 309 is coupled to the least significant bit of the V-BITS input, and a second select input (S1) of multiplexer 309 is coupled to the most significant bit of the V-BITS input. In operation, the output of multiplexer 309 is set to zero when the V-BITS value is either zero or 1. The output of multiplexer 309 is set to the PFVM value provided at the output of And gate 302, when the V-BITS value is set to either 2 or 3.

The output of sign extender 305 is coupled to the input of inverter 307, which has an output coupled to a first input of And gate 308. The second input of And gate 308 is coupled to the output of And gate 302, which provides PFVM. The output of And gate 308 is coupled to a first data input (D0) of multiplexer 310, and the output of multiplexer 309 is coupled to a second data input (D1) of multiplexer 310. A select input of multiplexer 310 is coupled to the most significant bit of QE. In operation, multiplexer 310 provides the PFVM value from the output of And gate 302, when the most significant bit of QE is equal to zero. When the most significant bit of QE is equal to 1, the output of multiplexer 310 is set as follows:

- The PFVM value provided at the output of And gate 302, when the V-BITS value equals 2 or 3; else
- Zero, when the V-BITS value equals 0 or 1.

Pixel component error value QE is coupled to a first input of And gate 311, and the output of multiplexer 310 is coupled to a second input of And gate 311. The output of And gate 311 is coupled to a first input of Or gate 315.

The PFVM output of And gate 302 is also coupled to the input of inverter 306, which has an output coupled to the first input of And gate 312. A second input of And gate 312 is coupled to the VMASK value. The output of And gate 312 is coupled to a first input of Or gate 313, which has a second input coupled to the output of sign extender 305.

Multiplexer 314 has a select input coupled to the most significant bit of QE. A first data input (D0) of multiplexer 314 is coupled to hexadecimal value 0000, and a second data input (D1) of multiplexer 314 is coupled to the output of Or gate 313. In operation, the output of multiplexer 314 provides hexadecimal value 0000, when the most significant bit of QE is zero. If the most significant bit of QE is 1, then the output of multiplexer 314 is equal to hexadecimal value 1FFF. The output of multiplexer 314 is coupled to the second data input of Or gate 315, which provides

the VERR value.

In operation, mask circuit 292 operates to provide the following VERR values:

- When the most significant bit of QE is 1, then the VERR value is equal to hexadecimal value 1FFF; and
- When the most significant bit of QE is equal to zero, then the VERR value is equal to the PFVM output of And gate 302 Anded with QE.

Returning to Fig. 7, it is seen at the vertical error circuit output (VERR) is coupled to the input of shifter 214. The 8 least significant bits of VERR are provided to shifter 214. Shifter 214 employs the V-BITS and V-SHIFT signals to convert VERR into EDVV. The V-BITS signal identifies whether EDVV will have a sign bit. If V-BITS is equal to zero, EDVV will be equal to zero. If V-BITS is equal to 1, then EDVV will not contain the sign bit. In this instance, the VERR bit corresponding to the V-SHIFT value is loaded into the EDVV value and padded by 2 leading zeros. For example, if V-SHIFT is equal to 3, then bit [3] of the VERR value provided to the input of shifter 214 is padded by 2 leading zeroes and used as EDVV.

When V-BITS is equal to 2 or 3, the EDVV value includes a sign bit as the most significant bit. In this instance, shifter 214 sets the most significant bit of EDVV equal to the most significant bit of QE. For V-BITS equal to 2, the least significant bit of EDVV is set to equal the VERR bit corresponding to the V-SHIFT. The next least significant bit of EDVV is also equal to the most significant bit of QE to provide sign extension.

For V-BITS equal to 3, the least significant bit of EDVV is equal to the VERR bit corresponding to the V-SHIFT value, and the next least significant EDVV bit is equal to the [V-SHIFT +1] bit of the VERR value. For example, if V-SHIFT is equal to 3, and V-BITS is equal to 3, then bit [3] of the VERR value provided to the input of shifter 214 is selected to fill the least significant bit of EDVV. The next least significant bit of EDVV is set equal to bit [4] of VERR. The following EDVV bit is the most significant bit and is set to the most significant bit of QE.

Horizontal error circuit 216 (Fig. 7) employs all of the inputs of temporal error circuit 204 and vertical error circuit 212 to generate a horizontal dimensional error diffusion value (EDVH). In one embodiment of the present invention, this is achieved by subtracting the expanded temporal dimensional error diffusion value (TERR) and the expanded vertical dimensional error diffusion value (VERR) from the pixel component error value (QE). In one embodiment, this subtraction is achieved by substantially duplicating the functionality of temporal error circuit 204 and vertical

error circuit 212, as described above, within the horizontal error circuit 216. The resulting expanded dimensional error diffusion values are then subtracted from the pixel component error value QE.

Fig. 14 illustrates a block diagram of circuitry for horizontal error circuit 216 (Fig. 7) in one embodiment of the present invention. Perturbation factor circuit 400 receives the R2 and T-PERTURB inputs and provides a temporal perturbation factor (PFT) to mask circuit 408. Bit mask circuit 402 receives the T-SHIFT and T-BITS inputs and provides a TMASK signal to mask circuit 408. Bit mask circuit 404 receives the V-BITS and V-SHIFT inputs and provides a VMASK signal to mask circuit 408. Perturbation factor circuit 406 receives the R3 and V-PERTURB inputs and provides a vertical perturbation factor (PFV) to mask circuit 408. Circuitry for implementing perturbation factor circuit 400, bit mask circuit 402, bit mask circuit 404, and perturbation factor circuit 406 is the same as the circuitry shown above in Figs. 10(a)-(c) and Figs. 13(a)-(c) for perturbation factor circuit 230, bit mask circuit 234, bit mask circuit 294, and perturbation factor circuit 290, respectively.

Mask circuit 408 employs PFT, TMASK, QE, VMASK, PFV, T-BITS, and V-BITS to generate EDVH. In one embodiment of the present invention, EDVH is equal to the pixel component error value (QE) minus the sum of the TERR value generated by temporal error circuit 204 and the VERR value generated by vertical error circuit 212.

Fig. 15 illustrates circuitry employed in one embodiment of the invention to form mask circuit 408, so that EDVH is the difference between QE and the sum of TERR and VERR. PFT is coupled to a first input of And gate 410, which has a second input coupled to receive TMASK. The output of And gate 410 provides a masked temporal perturbation factor (PFTM), which is coupled to third (D2) and fourth (D3) data inputs of multiplexer 412. The first (D0) and second (D1) data inputs of multiplexer 412 are coupled to hexadecimal value 0000. The first select input (S0) of multiplexer 412 is coupled to the least significant bit of the T-BITS input, and the second select input (S1) of multiplexer 412 is coupled to the most significant bit of the T-BITS signal. The output of multiplexer 412 is coupled to a second data input (D1) of multiplexer 430, which has a first data input (D0) coupled to hexadecimal value 0000. A select input of multiplexer 430 is coupled to the most significant bit of QE. The output of multiplexer 430 is coupled to Or gate 442.

Multiply by 2 circuit 460 has an input coupled to TMASK and an output coupled to an input of inverter 414, which has an output coupled to a first input of

And gate 416. A second input of And gate 416 is coupled to TMASK, and the output of And gate 416 is coupled to third (D2) and fourth (D3) data inputs of multiplexer 432. The first (D0) and second (D1) data inputs of multiplexer 432 are coupled to hexadecimal value 0000. A first select input (S0) of multiplexer 432 is coupled to the least significant bit of the T-BITS input, and a second select input (S1) of multiplexer 432 is coupled to the most significant bit of the T-BITS input. The output of multiplexer 432 is coupled to a first input of Or gate 448.

Multiplexer 418 has a first data input (D0) coupled to hexadecimal value 0000, and second (D1), third (D2), and fourth (D3) data inputs coupled to the PFTM output of And gate 410. A first select input (S0) of multiplexer 418 is coupled to a least significant bit of the T-BITS input, and a second select input (S1) of multiplexer 418 is coupled to the most significant bit of the T-BITS input. The output of multiplexer 418 is coupled to a first data input (D0) of multiplexer 434, which has a second data input coupled to hexadecimal value 0000. A select input of multiplexer 434 is coupled to the most significant bit of QE. An output of multiplexer 434 is coupled to a first data input of And gate 446.

The vertical perturbation factor (PFV) is coupled to a first input of And gate 420, which has a second input coupled to receive VMASK. The output of And gate 420 provides a masked vertical perturbation factor (PFVM), which is coupled to the third (D2) and fourth (D3) data inputs of multiplexer 422. The first (D0) and second (D1) data inputs of multiplexer 422 are coupled to hexadecimal value 0000. A first select input (S0) of multiplexer 422 is coupled to the least significant bit in the V-BITS input, and a second select input (S1) of multiplexer 422 is coupled to the most significant bit in the V-BITS input. The output of multiplexer 422 is coupled to a second data input (D1) of multiplexer 436, which has a first data input (D0) coupled to hexadecimal value 0000. A select input of multiplexer 436 is coupled to the most significant bit of QE. The output of multiplexer 436 is coupled to the second input of Or gate 442.

Multiply by 2 circuit 462 has an input coupled to VMASK and an output coupled to an input of inverter 426, which has an output coupled to a first data input of And gate 424. A second data input of And gate 424 is coupled to receive VMASK, and an output of And gate 424 is coupled to the third (D2) and fourth (D3) data inputs of multiplexer 438. The first (D0) and second (D1) data inputs of multiplexer 438 are coupled to hexadecimal value 0000. A first select input (S0) of multiplexer 438 is coupled to the least significant bit of the V-BITS input, and a

second select input (S1) of multiplexer 438 is coupled to the most significant bit of the V-BITS input. An output of multiplexer 438 is coupled to a second input of Or gate 448.

Multiplexer 428 has a first data input (D0) coupled to hexadecimal value 0000, and second (D1), third (D2), and fourth (D3) data inputs coupled to the PFVM output of And gate 420. A first select input (S0) of multiplexer 428 is coupled to the least significant bit of the V-BITS input, and a second select input (S1) of multiplexer 428 is coupled to the most significant bit of the V-BITS input. An output of multiplexer 428 is coupled to a first data input (D0) of multiplexer 440, which has a second data input (D1) coupled to hexadecimal value 0000. A select input of multiplexer 440 is coupled to the most significant bit of QE. An output of multiplexer 440 is coupled to a second input of And gate 446.

The output of Or gate 442 is coupled to a first input of Or gate 456. The output of And gate 446 is coupled to the input of inverter 452, which has an output coupled to a first data input of And gate 454. A second input of And gate 454 is coupled to pixel component error value QE. The output of And gate 454 is coupled to a second input of Or gate 456. The output of Or gate 448 is coupled to the second data input (D1) of multiplexer 450, which has a first data input (D0) coupled to hexadecimal value 0000. A select input of multiplexer 450 is coupled to the most significant bit of QE. The output of multiplexer 450 is coupled to a first input of adder 458. A second input of adder 458 is coupled to the output of Or gate 456. The output of adder 458 provides EDVH.

Fig. 15 illustrates circuitry used to form mask circuit 408 in one embodiment of the present invention. One with ordinary skill in the art will recognize that numerous other arrangements of circuitry can be developed to satisfy the functionality of mask circuit 408.

The foregoing detailed description of the invention has been presented for purposes of illustration and description. It is not intended to be exhaustive or to limit the invention to the precise form disclosed, and obviously many modifications and variations are possible in light of the above teaching. The described embodiments were chosen in order to best explain the principles of the invention and its practical application to thereby enable others skilled in the art to best utilize the invention in various embodiments and with various modifications as are suited to the particular use contemplated. It is intended that the scope of the invention be defined by the claims appended hereto.

CLAIMS

What is claimed is:

1. A method for processing image data, said method comprising the steps of:

(a) receiving a pixel component for a pixel;

(b) adding a first set of dimensional error diffusion values to said pixel component to generate a modified pixel component, wherein said first set of dimensional error diffusion values includes a first temporal dimensional error diffusion value, a first horizontal dimensional error diffusion value, and a first vertical dimensional error diffusion value; and

(c) generating a pixel component display value based on said modified pixel component.

2. The method of claim 1, wherein said step (c) includes the steps of:

identifying a number of bits to be included in said pixel component display value; and

selecting said number of bits from said modified pixel component.

3. The method of claim 1, further including the step of:

(d) generating a pixel component error value.

4. The method of claim 3, wherein said step (d) includes the steps of:

normalizing said pixel component display value to generate a normalized pixel component display value; and

subtracting said normalized pixel component display value for said modified pixel component display value.

5. The method of claim 4, wherein said step (d) further includes the step of:

subtracting a first dimensional error diffusion value from said modified pixel component, wherein said first dimensional error diffusion value is a value in said first set of dimensional error diffusion values added to said pixel component in said step (b).

6. The method of claim 5, wherein said first dimensional error diffusion value is a random number value.

7. The method of claim 3, further including the step of:

(e) generating a second set of dimensional error diffusion values.

8. The method of claim 7, wherein said step (e) includes the step of:

allocating said pixel component error value between a second temporal dimensional error diffusion value, a second vertical dimensional error diffusion value, and a second horizontal dimensional error diffusion value.

9. The method of claim 7, wherein said step (e) includes the steps of:

generating a second vertical dimensional error diffusion value;

generating a second temporal dimensional error diffusion value; and

generating a second horizontal dimensional error diffusion value.

10. The method of claim 9, wherein said step of generating a horizontal dimensional error diffusion value includes the steps of:

generating an expanded vertical dimensional error diffusion value;

generating an expanded temporal dimensional error diffusion value; and

subtracting a sum of said expanded vertical dimensional error diffusion value and said expanded temporal dimensional error diffusion value from said pixel component error value.

11. The method of claim 9, wherein said step of generating a second vertical dimensional error diffusion value includes the steps of:

generating a vertical bit mask;

generating a vertical perturbation factor; and

applying said vertical bit mask, said vertical perturbation factor, and said pixel component error value in a mask operation to obtain an expanded vertical dimensional error diffusion value.

12. The method of claim 11, wherein said step of generating a second vertical dimensional error diffusion value further includes the step of:

reducing the number of bits in said expanded vertical dimensional error

diffusion value to obtain said second vertical dimensional error diffusion value.

13. The method of claim 11, wherein said step of generating a vertical perturbation factor includes the step of:

selecting a value in response to a random number value.

14. The method of claim 10, wherein said step of generating said vertical bit mask includes the steps of:

selecting a mask bit pattern; and

setting bit locations of said mask bit pattern within a set of bits in response to a weighting value.

15. The method of claim 9, wherein said step of generating a second temporal dimensional error diffusion value includes the steps of:

generating a temporal bit mask;

generating a temporal perturbation factor; and

applying said temporal bit mask, said temporal perturbation factor, and said pixel component error value in a mask operation to obtain an expanded temporal dimensional error diffusion value.

16. The method of claim 15, wherein said step of generating a second temporal dimensional error diffusion value further includes the step of:

reducing the number of bits in said expanded temporal dimensional error diffusion value to obtain said second temporal dimensional error diffusion value.

17. The method of claim 15, wherein said step of generating a temporal perturbation factor includes the step of:

selecting a value in response to a random number value.

18. The method of claim 15, wherein said step of generating said temporal bit mask includes the steps of:

selecting a mask bit pattern; and

setting bit locations of said mask bit pattern within a set of bits in response to a weighting value.

19. A method for generating a set of dimensional error diffusion values, based on a pixel component error value, said method comprising the steps of:

(a) generating a vertical dimensional error diffusion value;

(b) generating a temporal dimensional error diffusion value; and

(c) generating a horizontal dimensional error diffusion value.

20. The method of claim 19, wherein said step of generating a vertical dimensional error diffusion value includes the steps of:

generating a vertical bit mask;

generating a vertical perturbation factor; and

applying said vertical bit mask, vertical perturbation factor, and said pixel component error value in a mask operation to obtain an expanded vertical dimensional error diffusion value.

21. The method of claim 20, wherein said step of generating a vertical dimensional error diffusion value further includes the step of:

reducing the number of bits in said expanded vertical dimensional error diffusion value to obtain said vertical dimensional error diffusion value.

22. The method of claim 20, wherein said step of generating a vertical perturbation factor includes the step of:

selecting a value in response to a random number value.

23. The method of claim 20, wherein said step of generating said vertical bit mask includes the steps of:

selecting a mask bit pattern; and

setting bit locations of said mask bit pattern within a set of bits in response to a weighting value.

24. The method of claim 20, wherein said step of generating a temporal dimensional error diffusion value includes the steps of:

generating a temporal bit mask;

generating a vertical perturbation factor; and

applying said temporal bit mask, temporal perturbation factor, and said pixel component error value in a mask operation to obtain an expanded temporal

dimensional error diffusion value.

25. The method of claim 24, wherein said step of generating a temporal dimensional error diffusion value includes the step of:

reducing the number of bits in said expanded temporal dimensional error diffusion value to obtain said temporal dimensional error diffusion value.

26. The method of claim 24, wherein said step of generating a temporal perturbation factor includes the step of:

selecting a value in response to a random number value.

27. The method of claim 24, wherein said step of generating said temporal bit mask includes the steps of:

selecting a mask bit pattern; and

setting bit locations of said mask bit pattern within a set of bits in response to a weighting value.

28. The method of claim 24, wherein said step (c) includes the step of:

subtracting a sum of said expanded vertical dimensional error diffusion value and said expanded temporal dimensional error diffusion value from said pixel component error value.

29. An image processor for transforming a pixel, said image processor including:

an adder coupled to receive a pixel component value of said pixel and a first set of dimensional error diffusion values, said adder further including an output for providing a sum of said pixel component value and values in said first set of dimensional error diffusion values, wherein said values include a first temporal dimensional error diffusion value, a first vertical dimensional error diffusion value, and a first horizontal dimensional error diffusion value; and

a quantizer coupled to said adder output to receive said sum, said quantizer having a display output for providing a pixel component display value based on said sum.

30. The image processor of claim 29, wherein said quantizer further

includes an error output for providing a pixel component error value based on said sum.

31. The image processor of claim 30, further including:

an error distributor circuit having an input coupleable to said quantizer error output to receive said pixel component error value, said error distributor circuit having a set of outputs to provide temporal dimensional error diffusion values, vertical dimensional error diffusion values, and horizontal dimensional error diffusion values.

32. The image processor of claim 31, wherein said error distributor circuit includes:

a temporal error circuit for providing expanded temporal dimensional error diffusion values;

a vertical error circuit for providing expanded vertical dimensional error diffusion values; and

a horizontal error circuit for providing horizontal dimensional error diffusion values.

33. The image processor of claim 32, wherein said temporal error circuit includes:

a perturbation factor circuit having an input coupled to receive a random number and an output to provide a temporal perturbation factor in response to said random number;

a bit mask circuit coupled to receive a temporal weighting value and an output coupled to provide a temporal bit mask in response to said temporal weighting value; and

a temporal mask circuit having inputs coupled to receive said temporal perturbation factor, said temporal bit mask, and said pixel component error value, said temporal mask circuit having an output for providing an expanded temporal dimensional error diffusion value in response to said temporal perturbation factor, said temporal bit mask, and said pixel component error value.

34. The image processor of claim 33, wherein said error distributor circuit further includes:

a temporal shifter having an input coupled to said temporal mask circuit

output to receive said expanded temporal dimensional error diffusion value and an input coupled to receive said temporal weighting value, said temporal shift register having an output for providing a temporal error diffusion value in response to said temporal weighting value, wherein said temporal dimensional error diffusion value has less bits than said expanded temporal dimensional error diffusion value.

35. The image processor of claim 34, wherein said vertical error circuit includes:

a perturbation factor circuit having an input coupled to receive a random number and an output to provide a vertical perturbation factor in response to said random number;

a bit mask circuit coupled to receive a vertical weighting value and an output coupled to provide a vertical bit mask in response to said vertical weighting value; and

a vertical mask circuit having inputs coupled to receive said vertical perturbation factor, said vertical bit mask, and said pixel component error value, said vertical mask circuit having an output for providing an expanded vertical dimensional error diffusion value in response to said vertical perturbation factor, said vertical bit mask, and said pixel component error value.

36. The image processor of claim 35, wherein said error distributor circuit further includes:

a vertical shifter having an input coupled to said vertical mask circuit output to receive said expanded vertical dimensional error diffusion value and an input coupled to receive said vertical weighting value, said vertical shift register having an output for providing a vertical error diffusion value in response to said vertical weighting value, wherein said vertical dimensional error diffusion value has less bits than said expanded vertical dimensional error diffusion value.

37. The image processor of claim 36, wherein said horizontal error circuit has an output providing a difference between said pixel component error value and a sum of said expanded temporal dimensional error diffusion value and said expanded vertical dimensional error diffusion value.

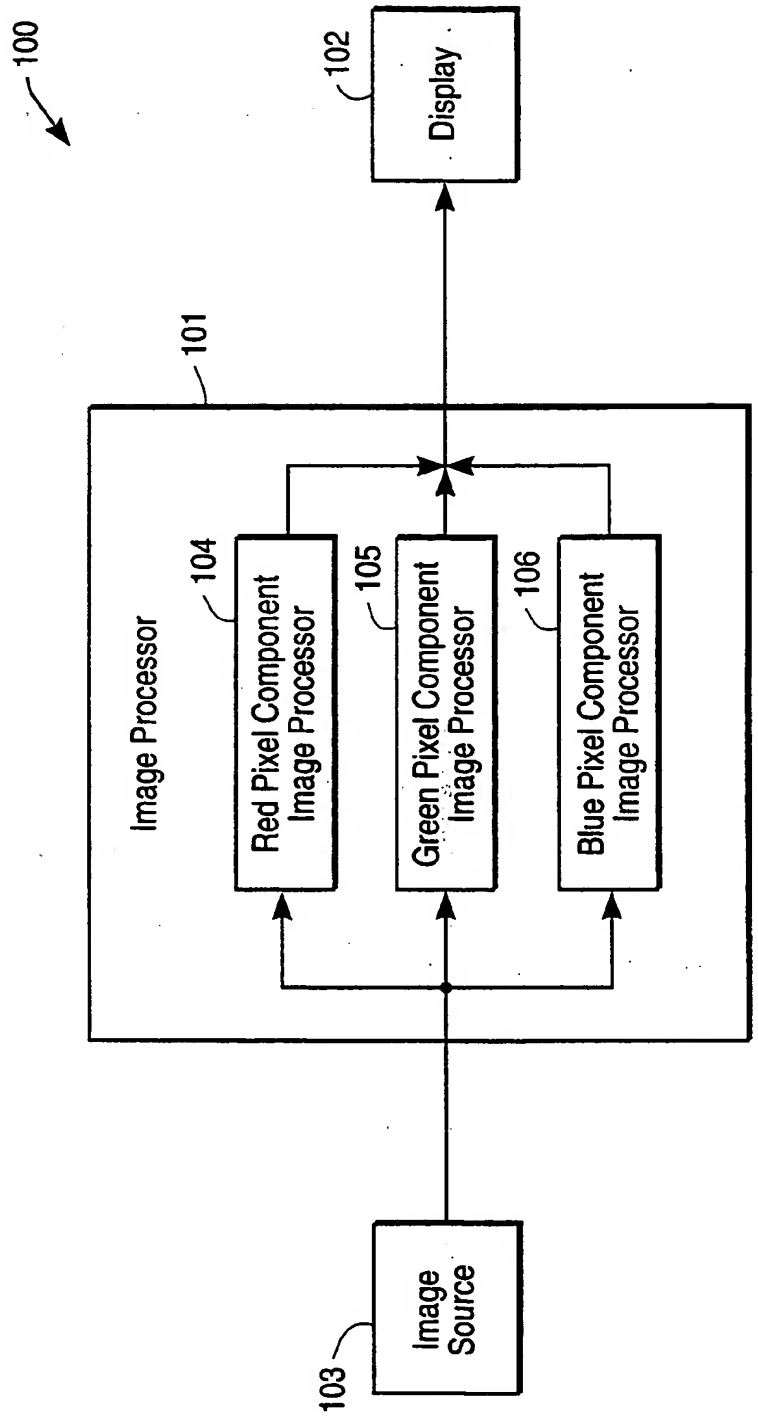
100
102
Display
101
Image Processor
104
Red Pixel Component Image Processor
105
Green Pixel Component Image Processor
106
Blue Pixel Component Image Processor
103
Image Source

FIG. 1

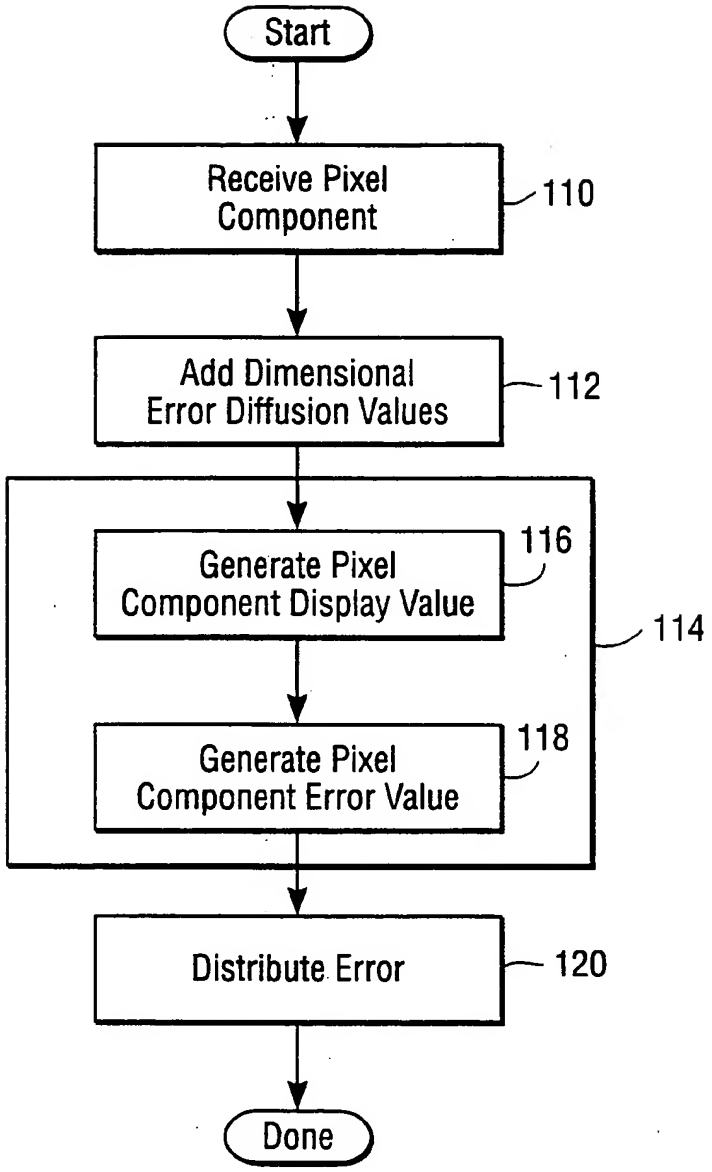
Start
Receive Pixel Component
110
Add Dimensional Error Diffusion Values
112
Generate Pixel Component Display Value
116
Generate Pixel Component Error Value
118
114
Distribute Error
120
Done

FIG. 2

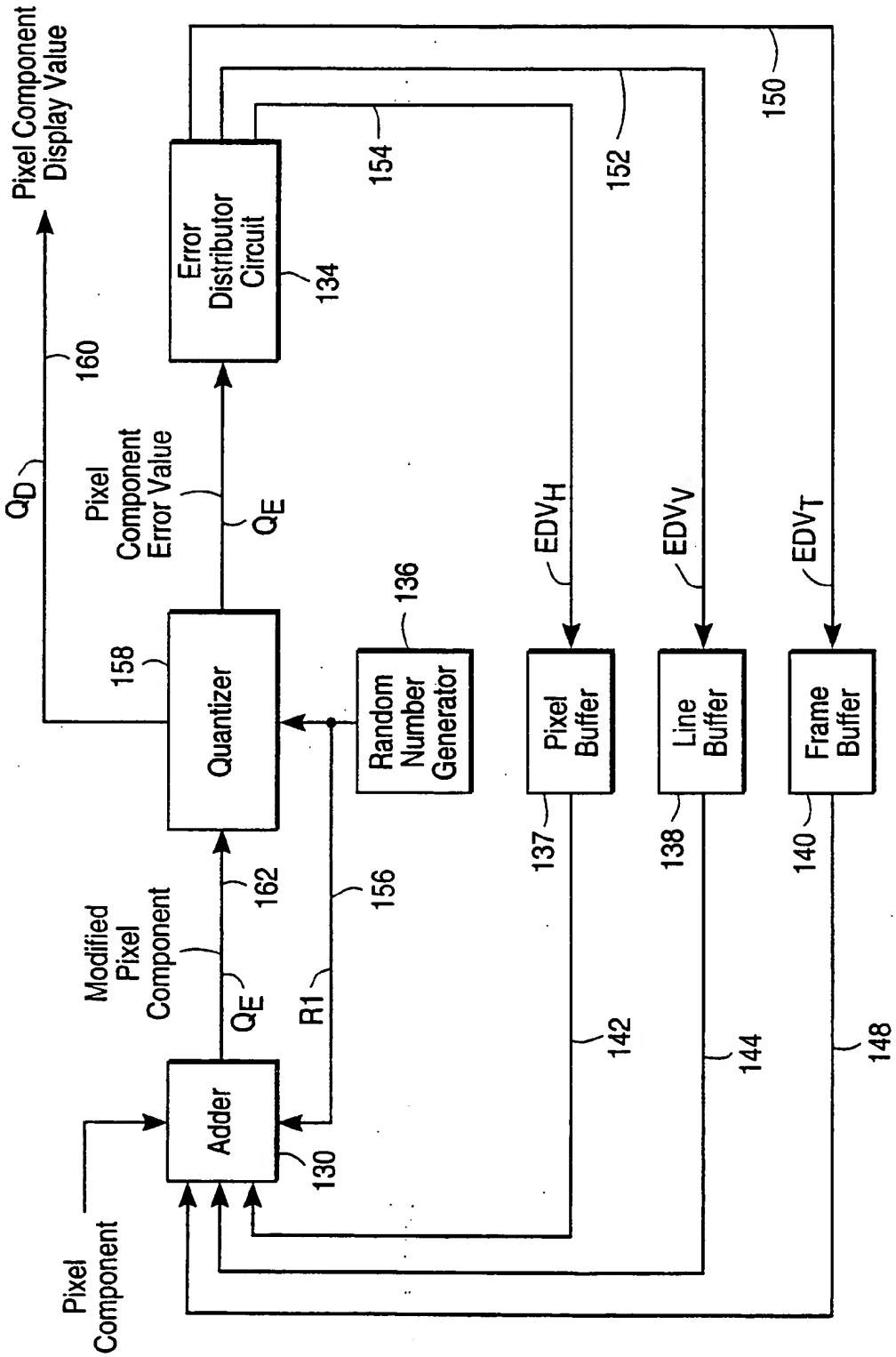
Pixel Component Display Value
Error Distributor Circuit
134
150
152
154
160
Q_D
Pixel Component Error Value
Q_E
Quantizer
158
Random Number Generator
136
EDV_H
EDV_V
EDV_T
Pixel Buffer
Line Buffer
Frame Buffer
137
138
140
Modified Pixel Component
Q_E
162
R1
156
Adder
130
Pixel Component
142
144
148

FIG. 3

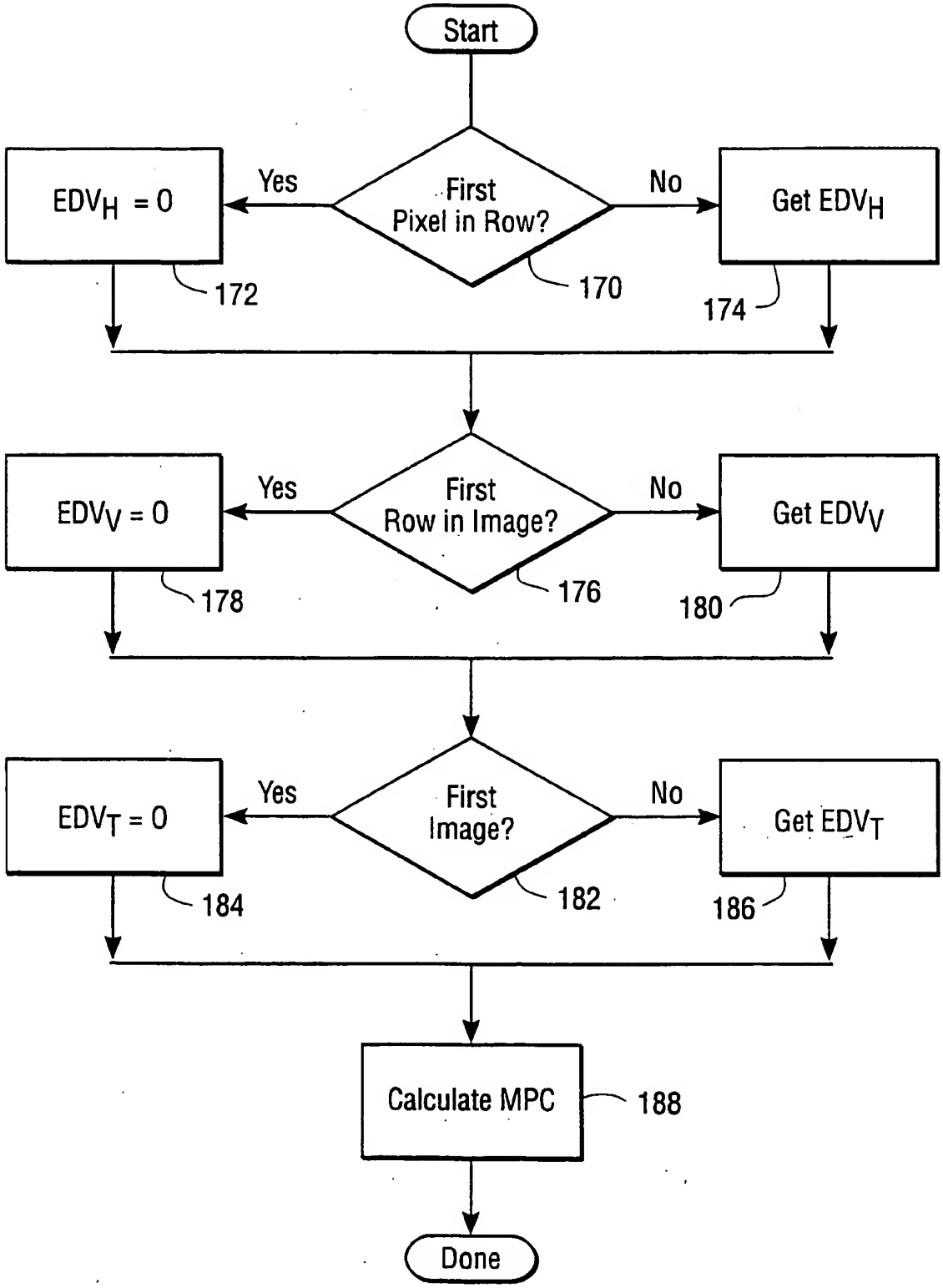
Start
First Pixel in Row?
Yes
No
EDV$_H$ = 0
Get EDV$_H$
172
170
174
First Row in Image?
EDV$_V$ = 0
Get EDV$_V$
178
176
180
First Image?
EDV$_T$ = 0
Get EDV$_T$
184
182
186
Calculate MPC
188
Done

FIG. 4

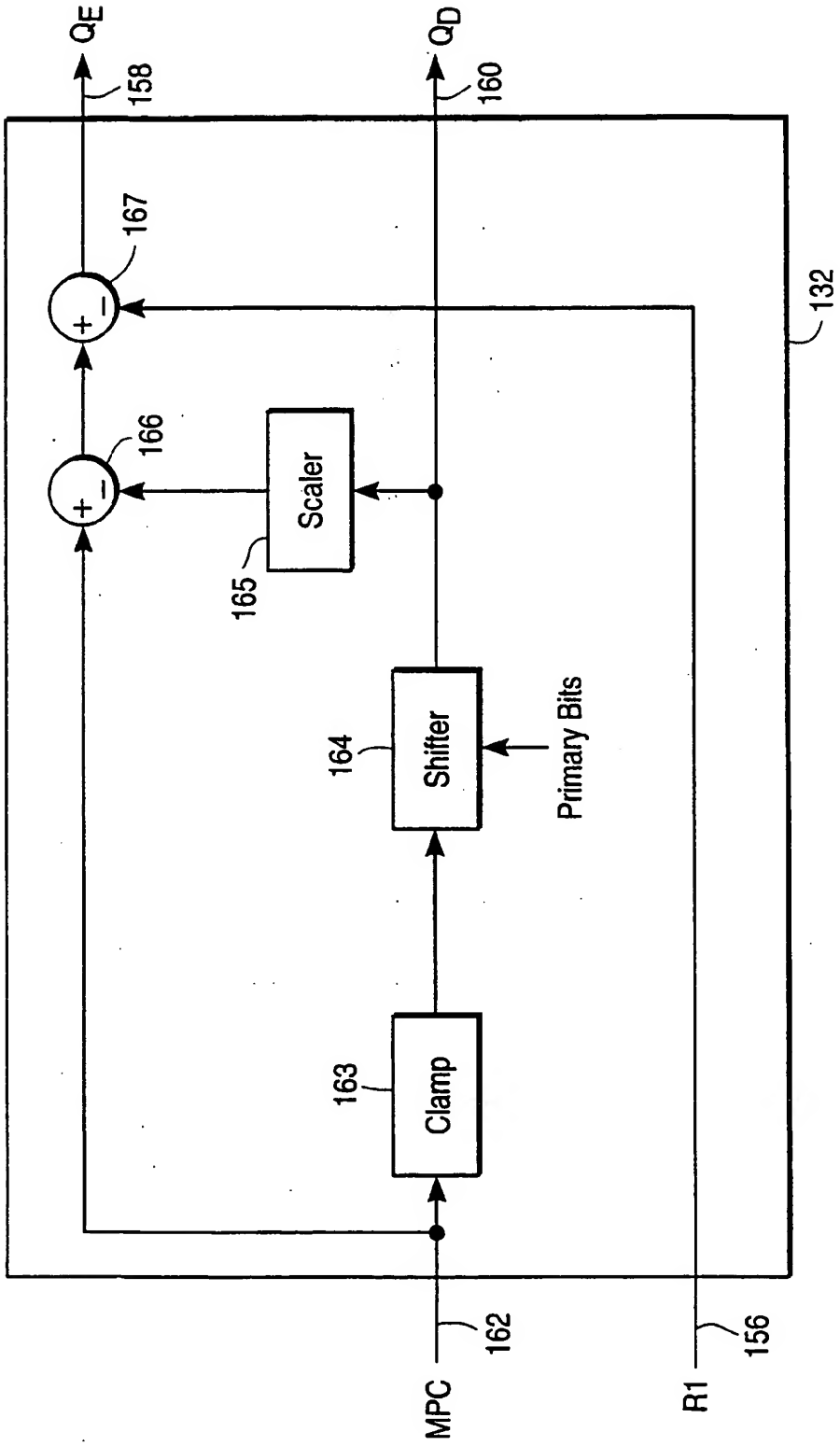
Q_E
158
Q_D
160
167
132
166
Scaler
165
164
Shifter
Primary Bits
163
Clamp
MPC
162
R1
156

FIG. 5

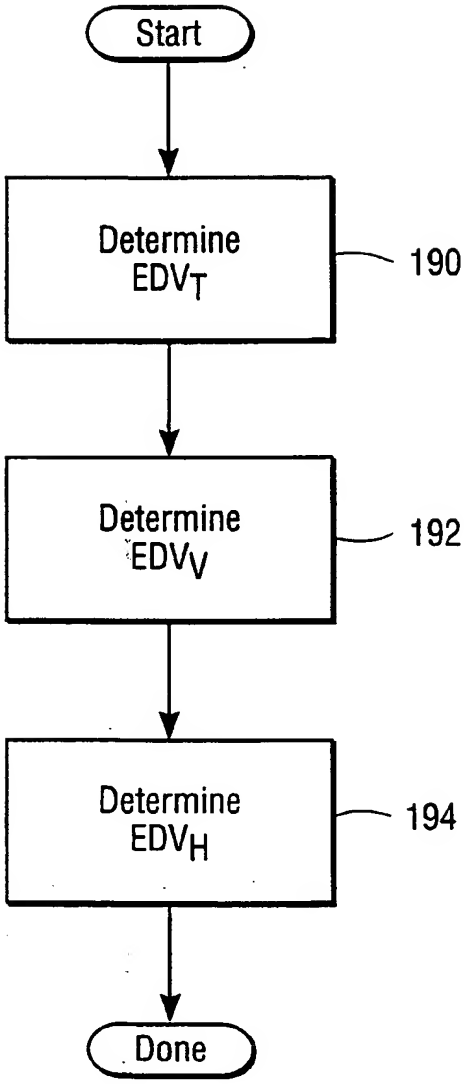
Start
Determine EDV_T
190
Determine EDV_V
192
Determine EDV_H
194
Done

FIG. 6

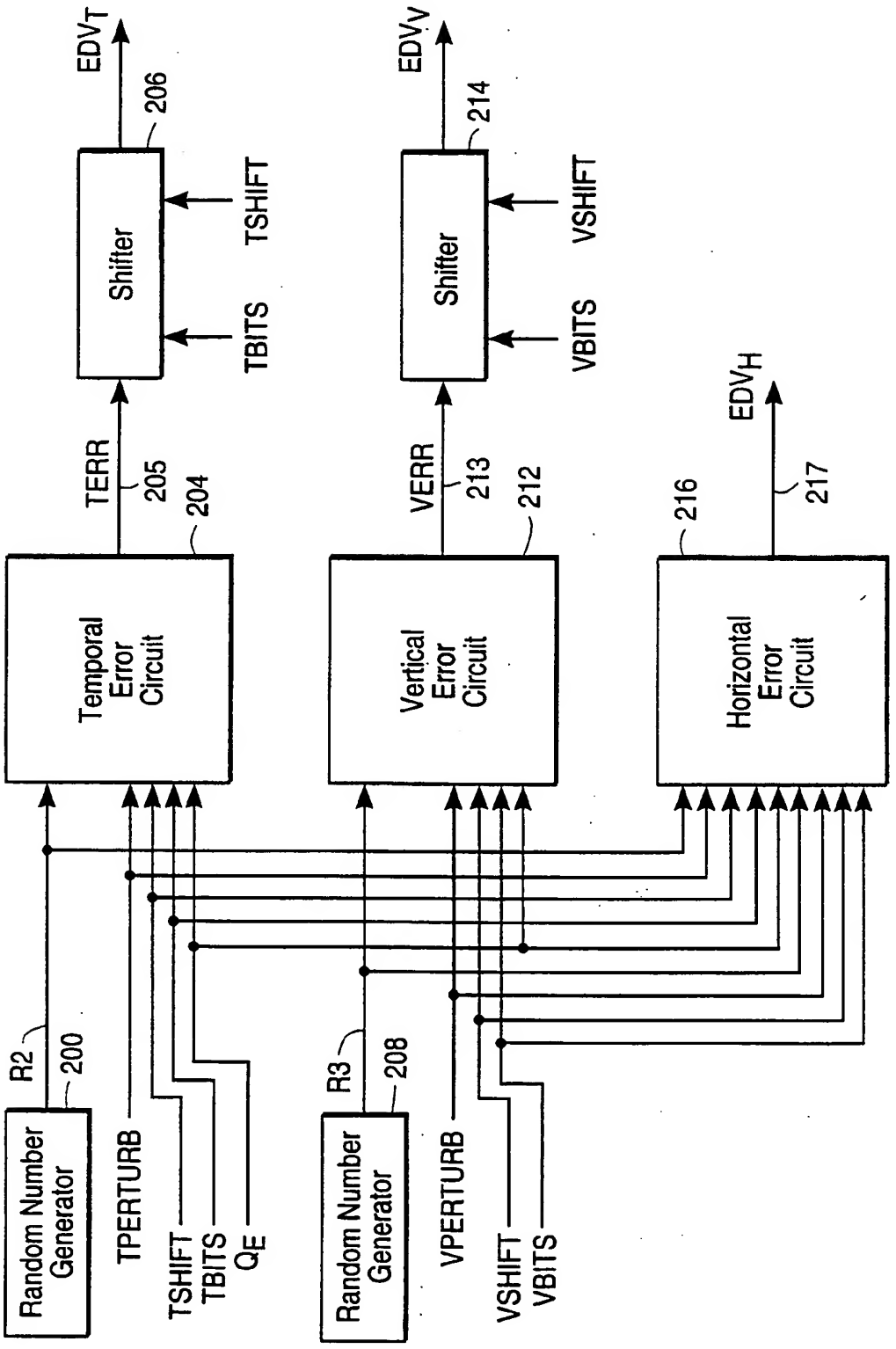
EDV$_T$
206
Shifter
TSHIFT
TBITS
EDV$_V$
214
Shifter
VSHIFT
VBITS
EDV$_H$
TERR
205
204
VERR
213
212
216
217
Temporal Error Circuit
Vertical Error Circuit
Horizontal Error Circuit
R2
200
Random Number Generator
TPERTURB
TSHIFT
TBITS
Q_E
R3
208
Random Number Generator
VPERTURB
VSHIFT
VBITS

FIG. 7

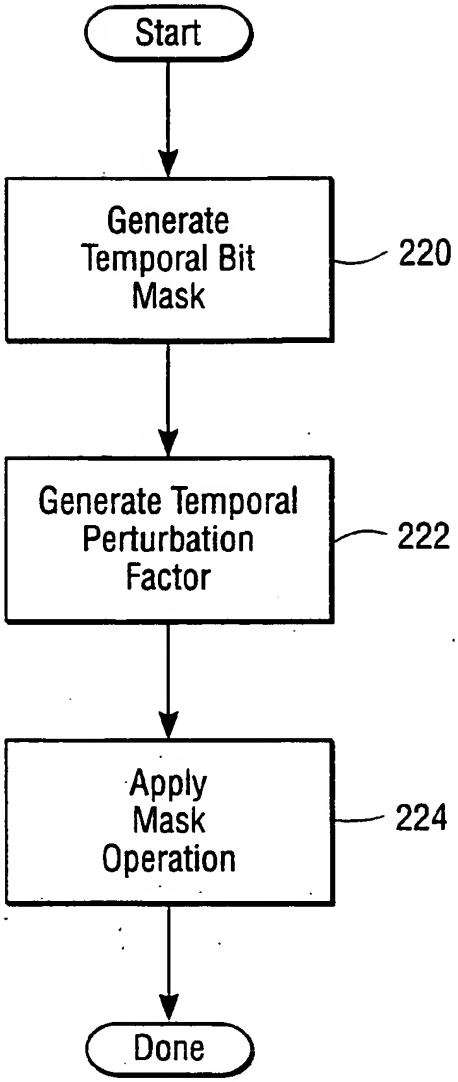
Start
Generate Temporal Bit Mask
220
Generate Temporal Perturbation Factor
222
Apply Mask Operation
224
Done

FIG. 8

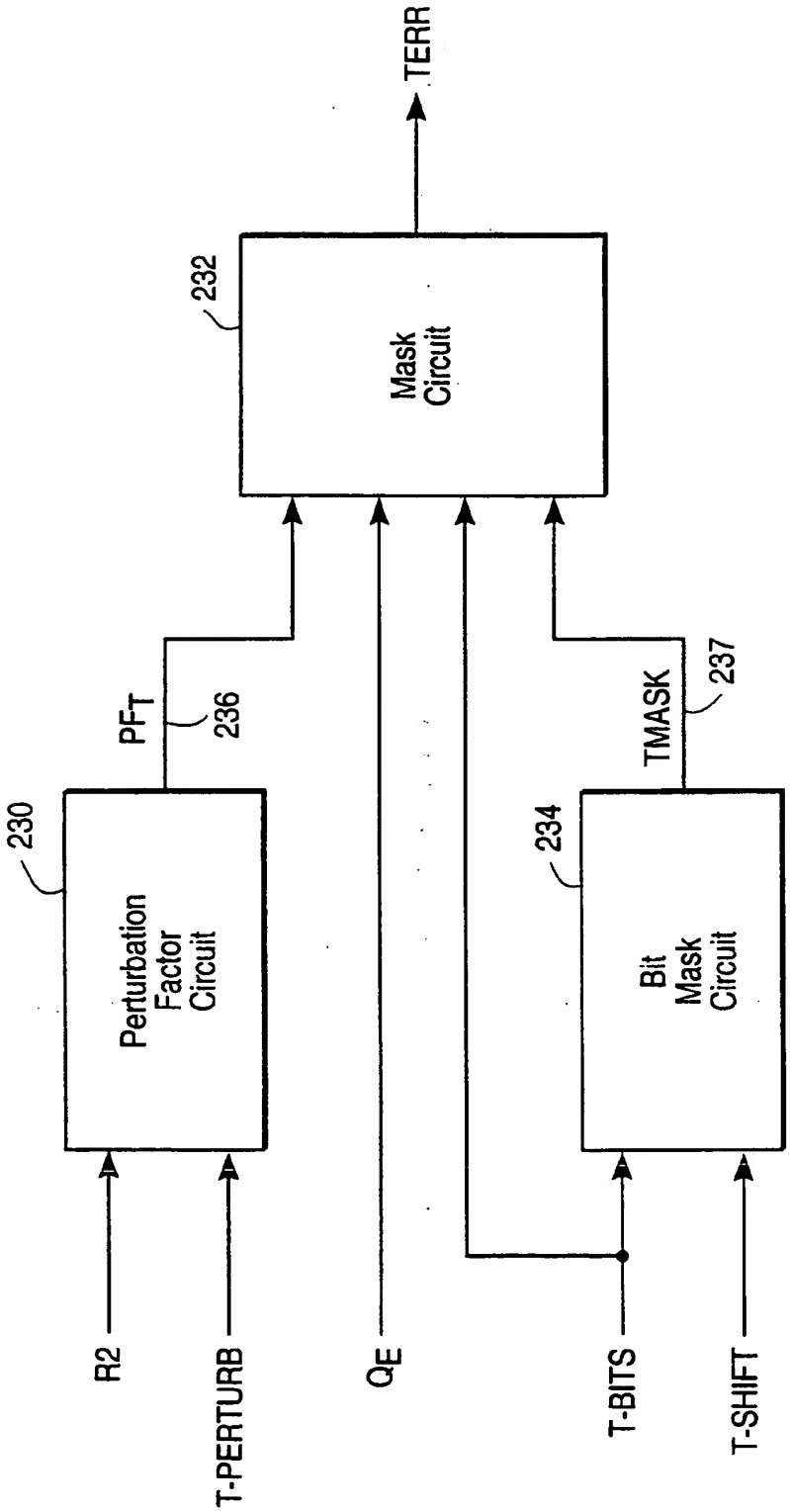
TERR
232
Mask Circuit
PFT
236
TMASK
237
230
Perturbation Factor Circuit
234
Bit Mask Circuit
R2
T-PERTURB
QE
T-BITS
T-SHIFT

FIG. 9

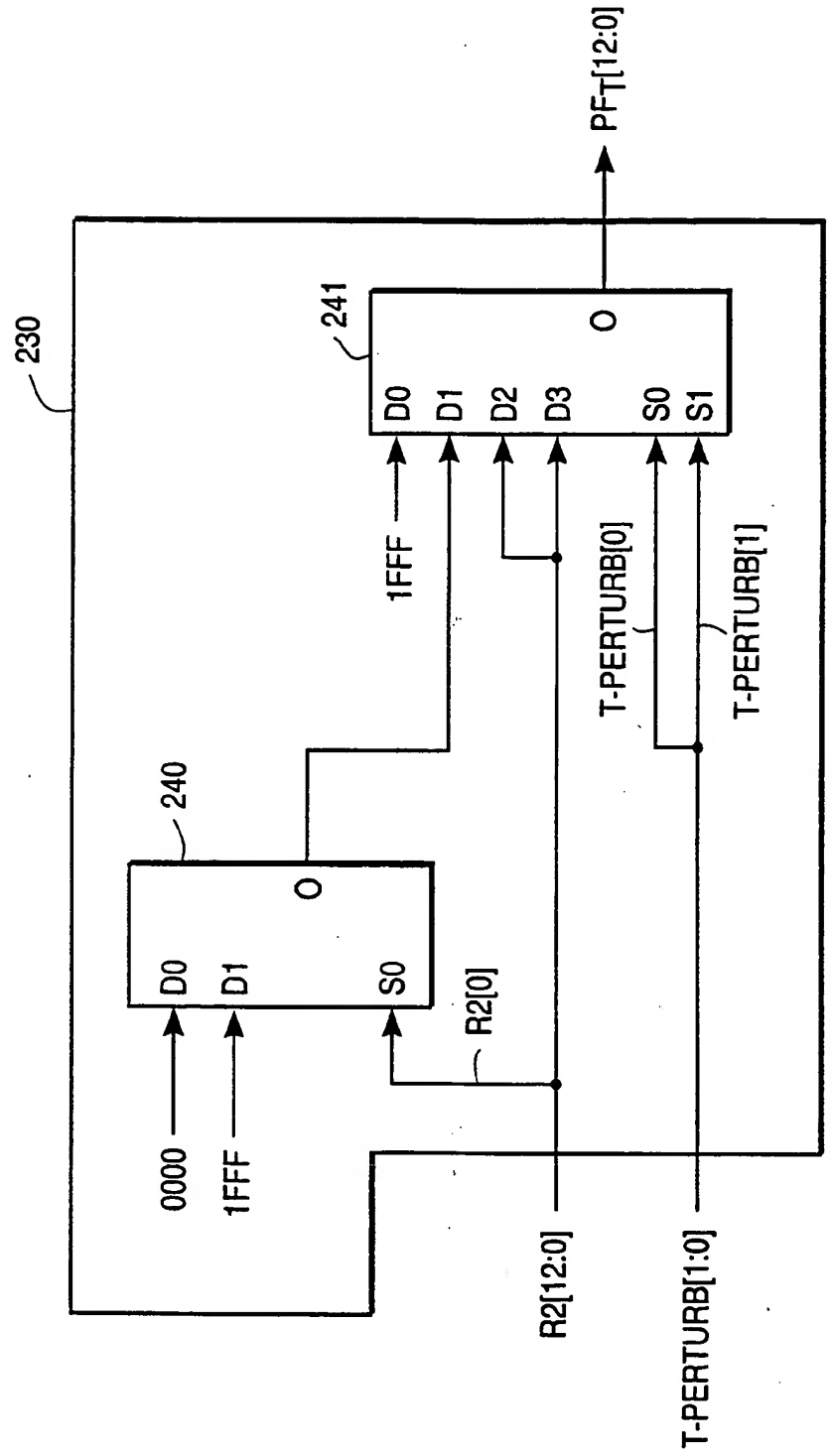
PF_T[12:0]
230
241
O
D0
D1
D2
D3
S0
S1
1FFF
T-PERTURB[0]
T-PERTURB[1]
240
O
D0
D1
S0
R2[0]
0000
1FFF
R2[12:0]
T-PERTURB[1:0]

FIG. 10A

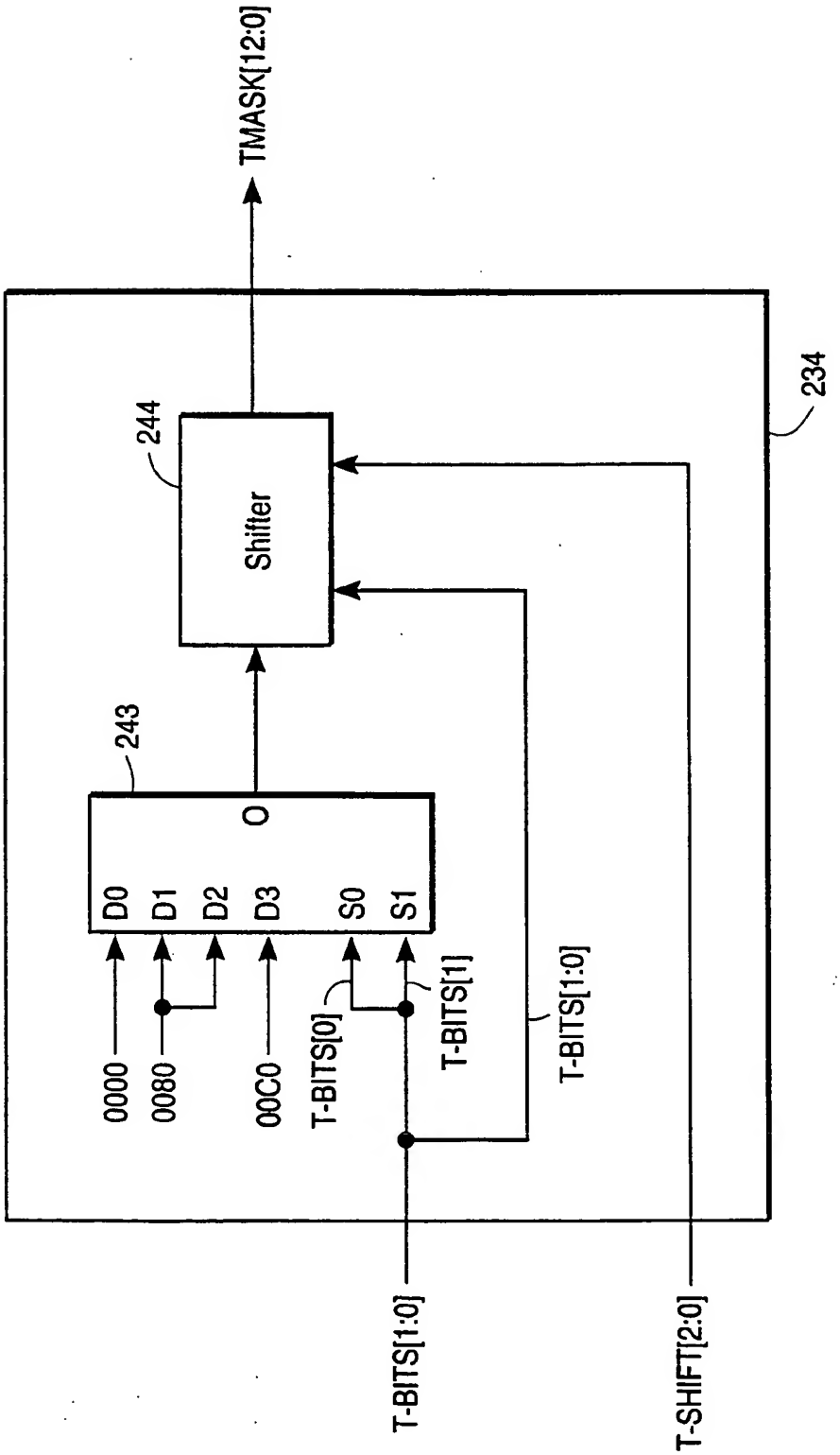
TMASK[12:0]
234
244
Shifter
243
O
D0
D1
D2
D3
S0
S1
0000
0080
00C0
T-BITS[0]
T-BITS[1]
T-BITS[1:0]
T-BITS[1:0]
T-SHIFT[2:0]

FIG. 10B

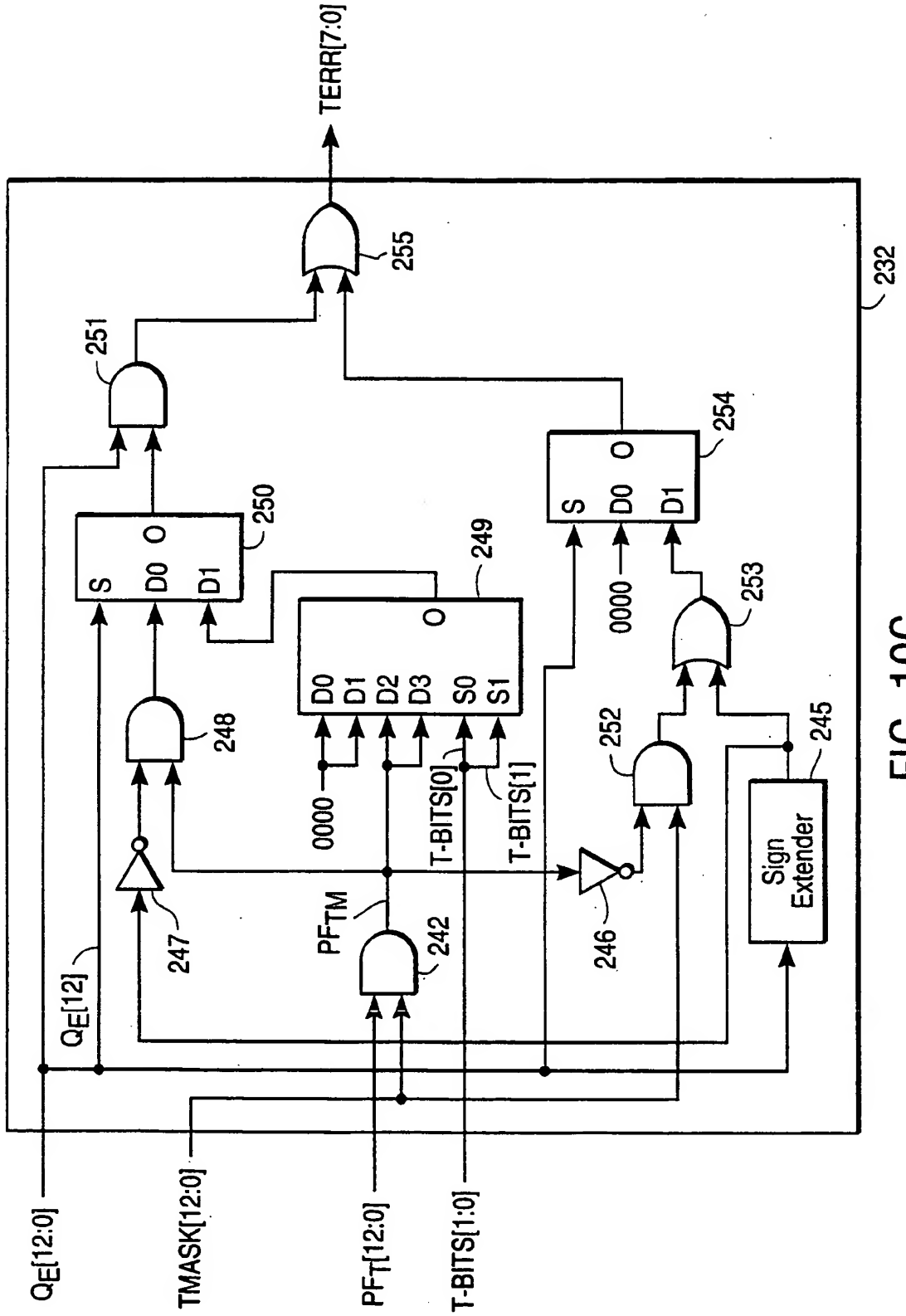
TERR[7:0]
255
232
251
254
250
249
253
248
252
245
247
246
242
Sign Extender
S
D0
D1
O
D0
D1
D2
D3
S0
S1
0000
0000
T-BITS[0]
T-BITS[1]
PF_TM
Q_E[12]
Q_E[12:0]
TMASK[12:0]
PF_T[12:0]
T-BITS[1:0]

FIG. 10C

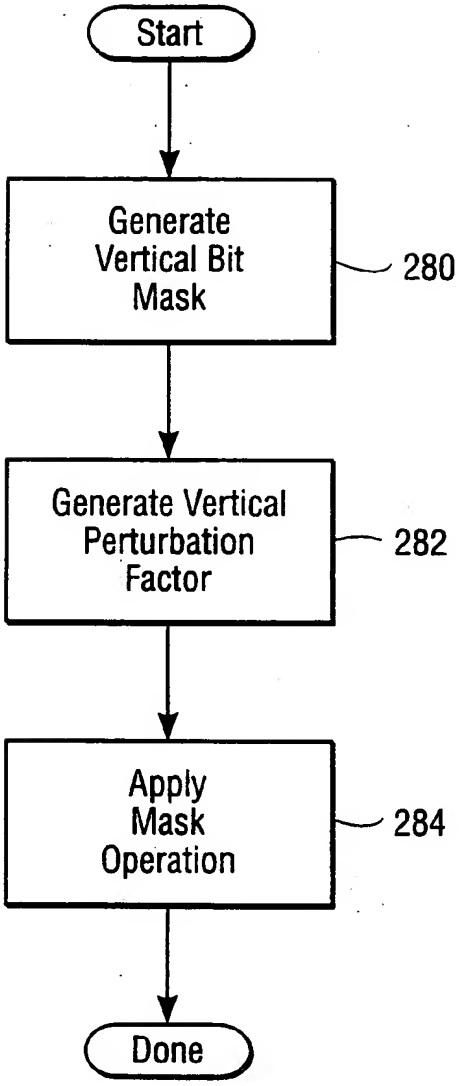
Start
Generate Vertical Bit Mask
280
Generate Vertical Perturbation Factor
282
Apply Mask Operation
284
Done

FIG. 11

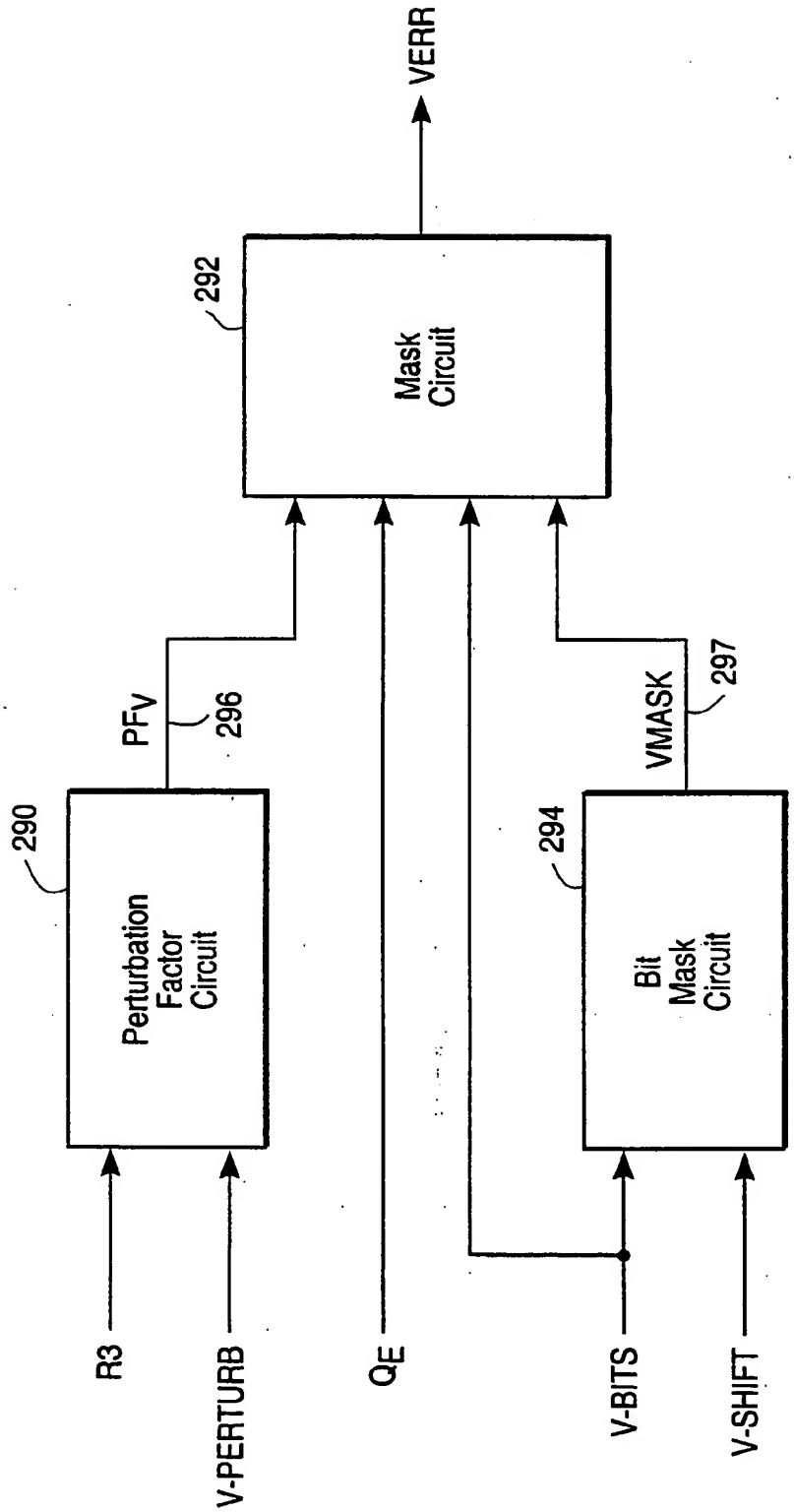
VERR
292
Mask Circuit
PFV
296
VMASK
297
290
Perturbation Factor Circuit
294
Bit Mask Circuit
R3
V-PERTURB
QE
V-BITS
V-SHIFT

FIG. 12

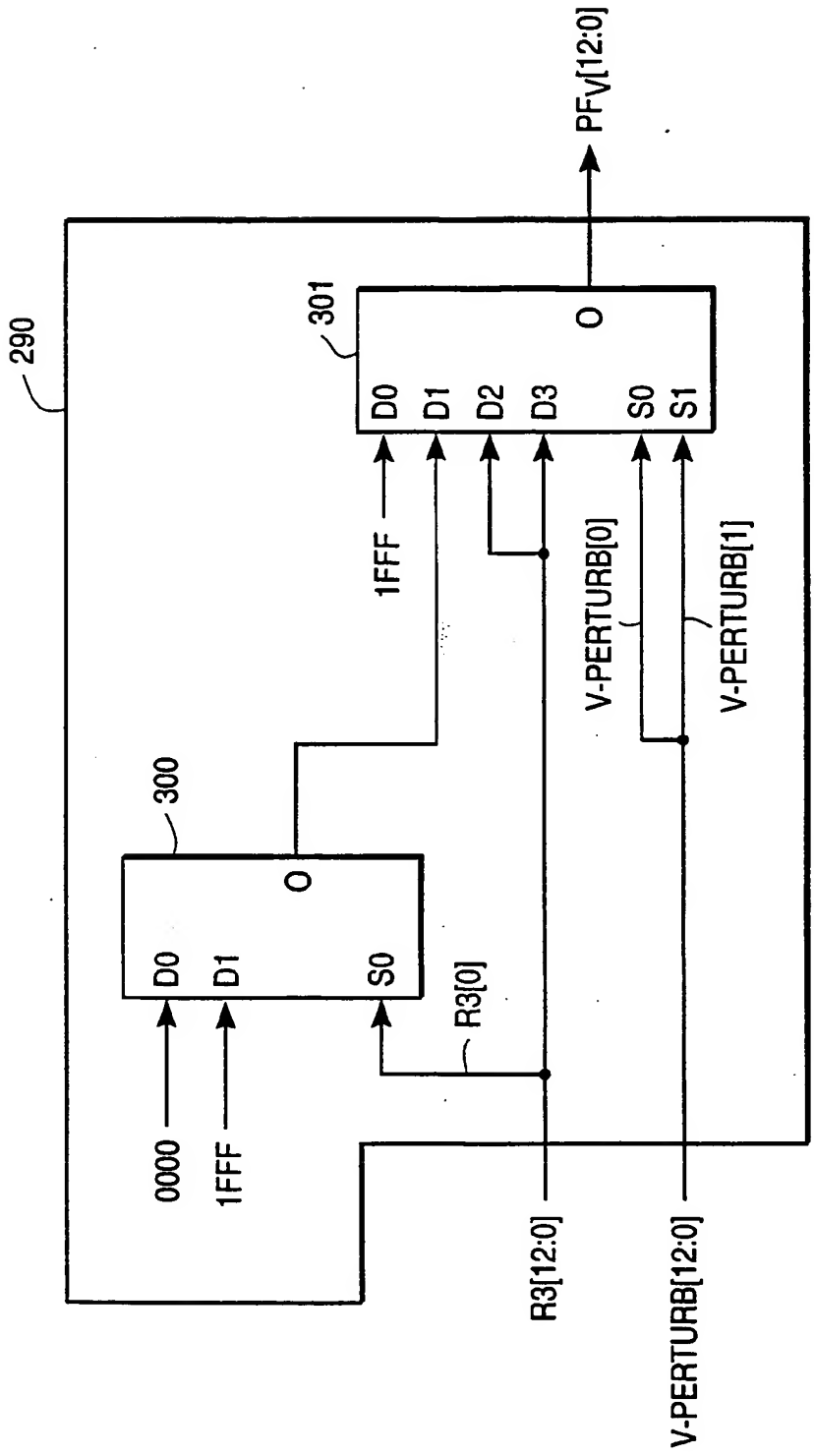
PFV[12:0]
290
301
O
D0
D1
D2
D3
S0
S1
1FFF
V-PERTURB[0]
V-PERTURB[1]
300
O
D0
D1
S0
R3[0]
0000
1FFF
R3[12:0]
V-PERTURB[12:0]

FIG. 13A

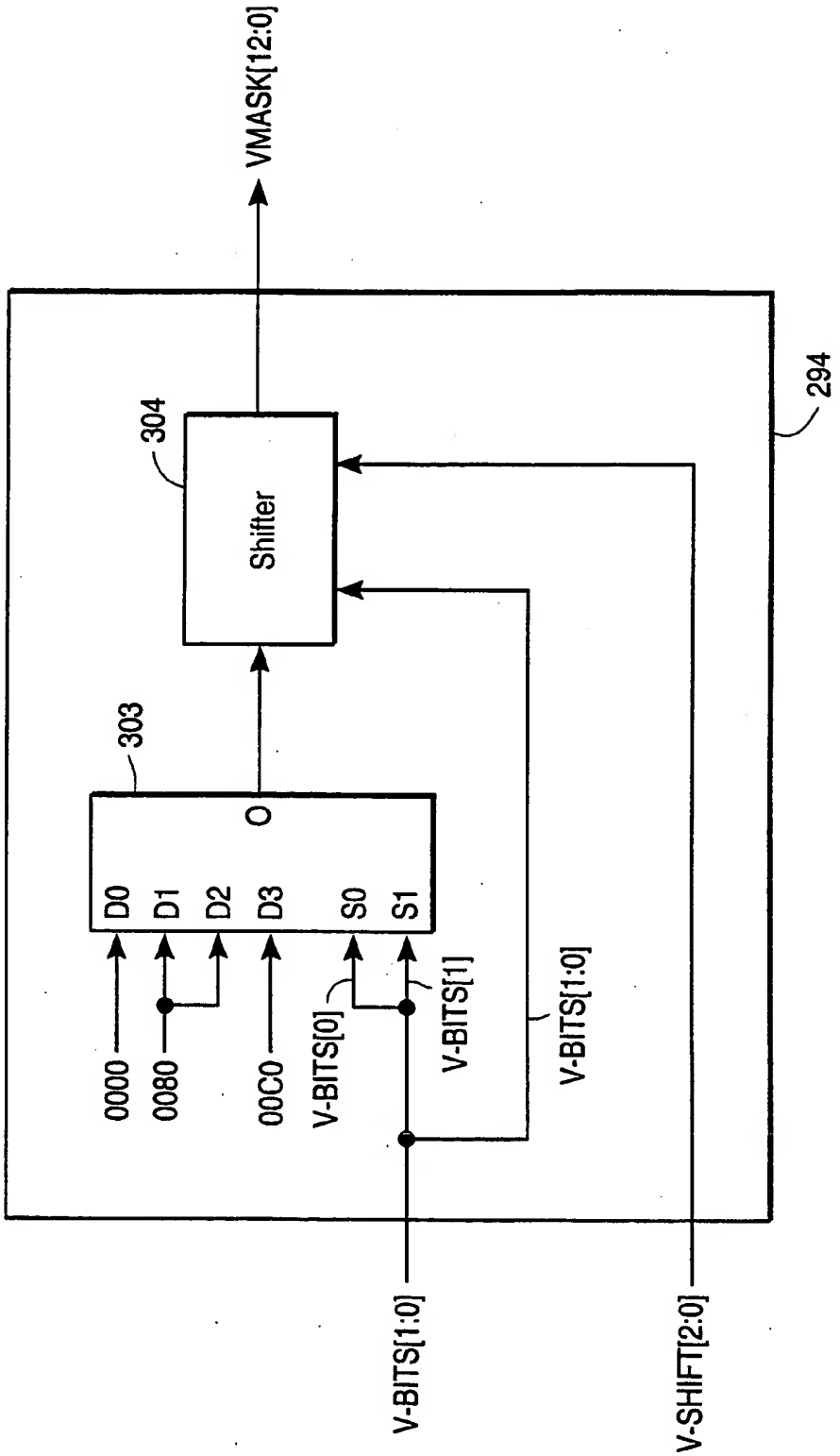
VMASK[12:0]
294
304
Shifter
303
O
D0
D1
D2
D3
S0
S1
0000
0080
00C0
V-BITS[0]
V-BITS[1]
V-BITS[1:0]
V-BITS[1:0]
V-SHIFT[2:0]

FIG. 13B

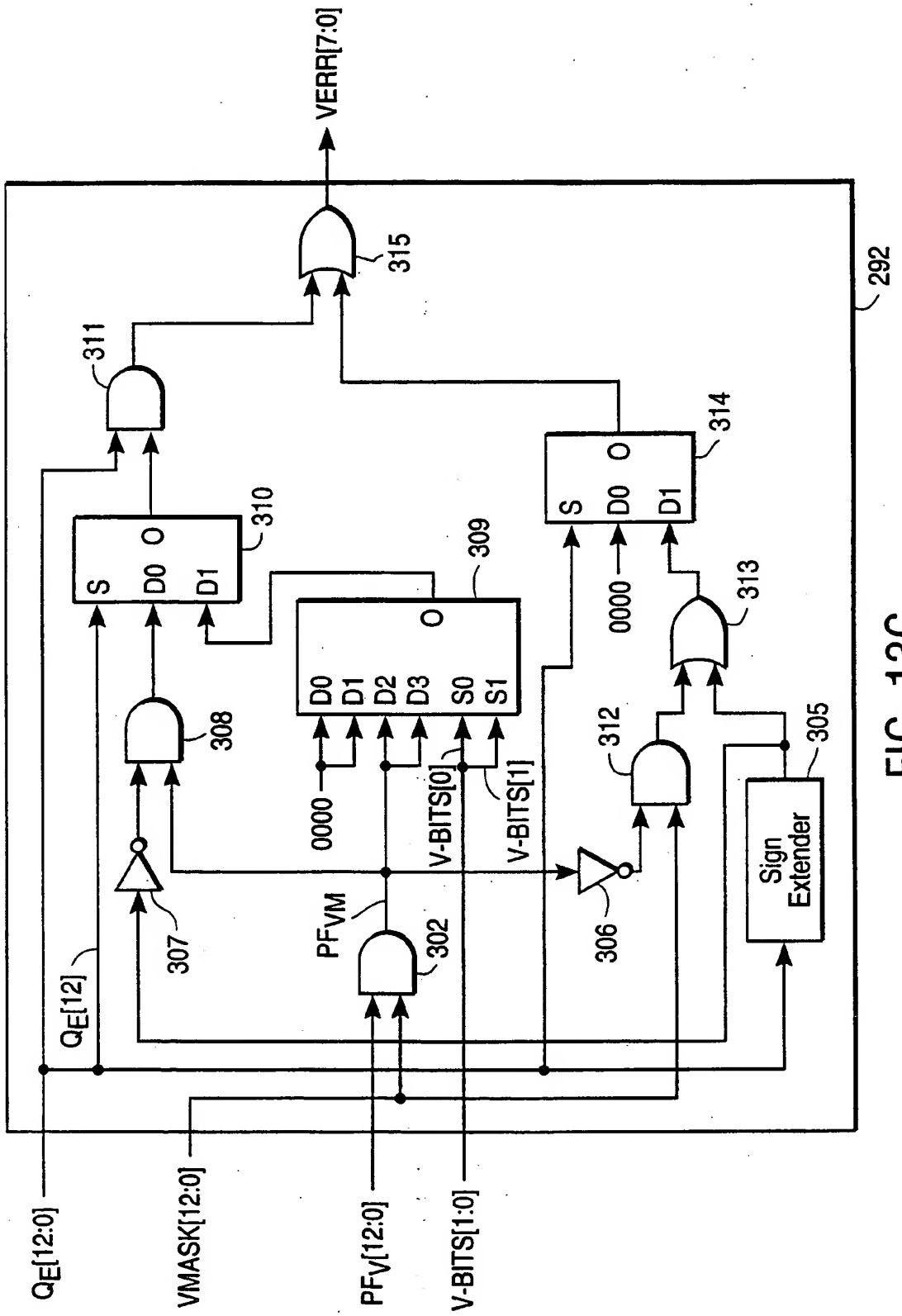
VERR[7:0]
315
292
311
314
310
309
313
308
312
305
307
306
302
S
D0
O
D1
D2
D3
S0
S1
0000
V-BITS[0]
V-BITS[1]
PFVM
Sign Extender
QE[12]
QE[12:0]
VMASK[12:0]
PFV[12:0]
V-BITS[1:0]

FIG. 13C

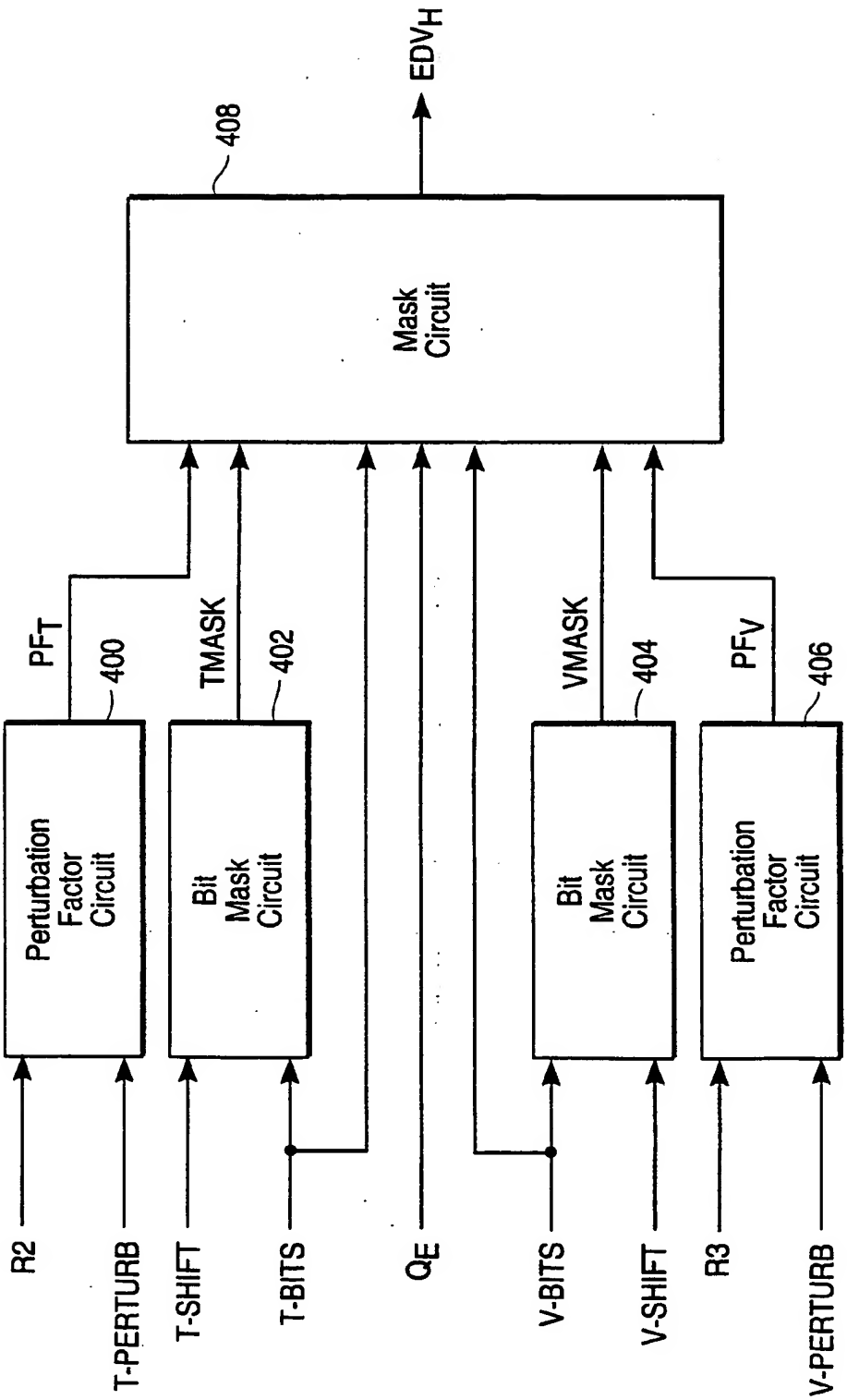
EDV_H
408
Mask Circuit
PF_T
400
TMASK
402
VMASK
404
PF_V
406
Perturbation Factor Circuit
Bit Mask Circuit
Bit Mask Circuit
Perturbation Factor Circuit
R2
T-PERTURB
T-SHIFT
T-BITS
Q_E
V-BITS
V-SHIFT
R3
V-PERTURB

FIG. 14

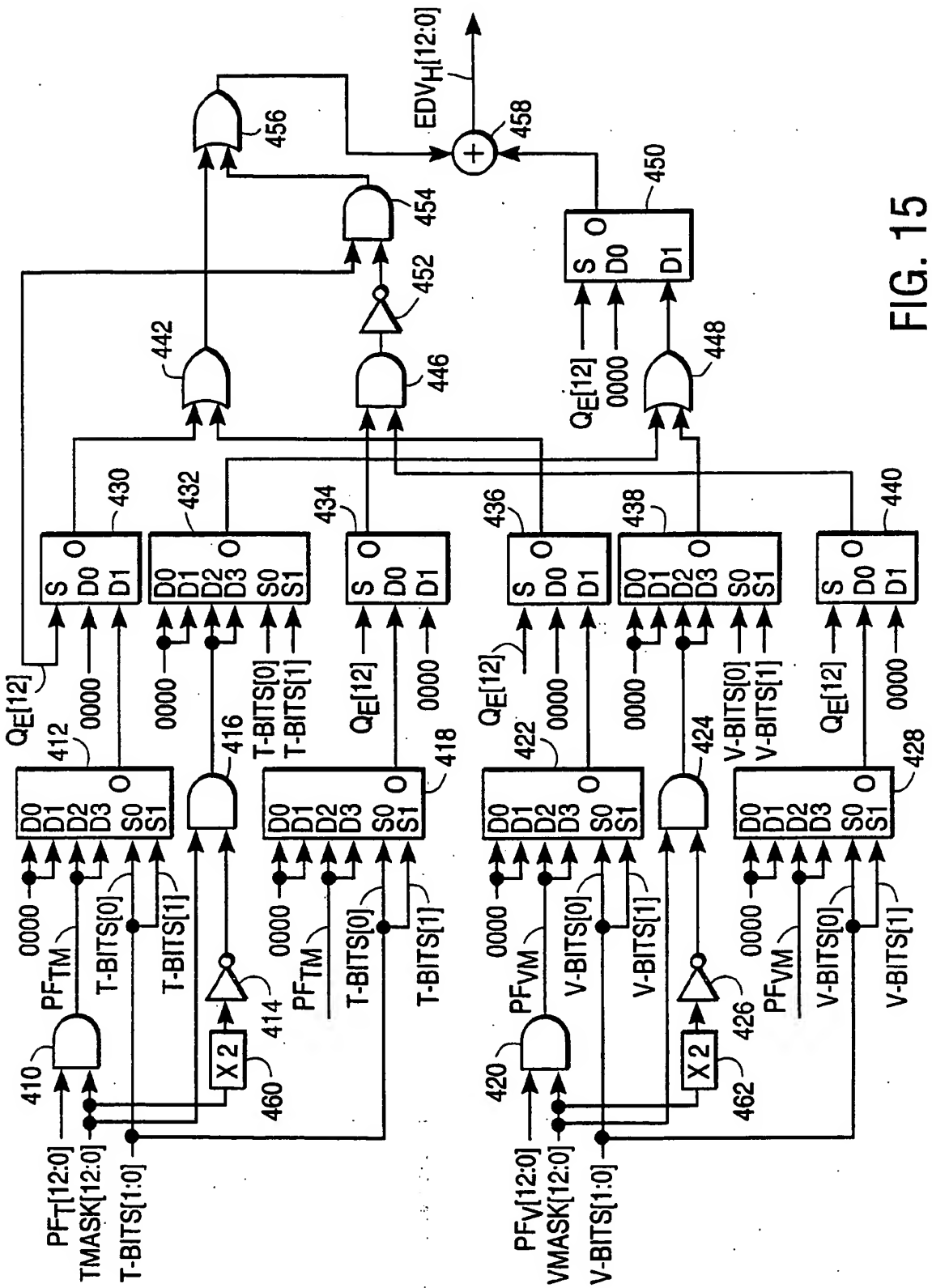
EDV_H[12:0]
456
458
454
452
450
442
446
448
Q_E[12]
0000
430
432
434
436
438
440
412
416
418
422
424
428
T-BITS[0]
T-BITS[1]
V-BITS[0]
V-BITS[1]
PF_TM
PF_VM
410
414
420
426
460
462
X 2
PF_T[12:0]
TMASK[12:0]
T-BITS[1:0]
PF_V[12:0]
VMASK[12:0]
V-BITS[1:0]

FIG. 15

INTERNATIONAL SEARCH REPORT

Inter. nal Application No
PCT/US 00/10567

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 G09G5/02

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 G09G

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
PAJ

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X Y	US 5 450 098 A (OZ) 12 September 1995 (1995-09-12) column 3, line 12 - line 38 see Abstract column 1, line 5 - line 30; figures 1B,3,4 column 1, line 67 -column 2, line 15 column 2, line 38 - line 54 column 5, line 18 -column 7, line 53 --- -/--	1-4,7-9, 19,29-32 5,6, 20-26, 33-37

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

° Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
10 August 2000	18/08/2000

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Corsi, F

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INTERNATIONAL SEARCH REPORT

International Application No
PCT/US 00/10567

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 5 404 176 A (LUM) 4 April 1995 (1995-04-04) see abstract column 1, line 48 - line 64; figures 1,4 column 2, line 39 - line 47 column 3, line 39 - line 62 column 4, line 55 -column 5, line 18 column 6, line 64 -column 8, line 13	5,6, 20-26, 33-37
X	US 5 596 349 A (KOBAYASHI ET AL.) 21 January 1997 (1997-01-21) see Abstract column 1, line 7 -column 2, line 18 column 6, line 11 -column 7, line 9; figure 2 column 28, line 7 -column 29, line 29; figures 16-24 column 31, line 60 -column 33, line 21 column 36, line 20 -column 37, line 45	1-3,7, 29,30
X	EP 0 573 174 A (CANON K.K) 8 December 1993 (1993-12-08) see abstract column 1, line 5 - line 12; figures 2-5,8 column 2, line 40 - line 47 column 5, line 14 -column 8, line 9 column 8, line 33 -column 9, line 38	1-3,7-9, 19,29-32
A	FR 2 752 633 A (FUJITSU LTD.) 27 February 1998 (1998-02-27) see abstract page 8, line 19 -page 9, line 23; figures 1,2,10A-15 page 14, line 10 -page 19, line 7	1-3,7-9, 19,29,30

Form PCT/ISA/210 (continuation of second sheet) (July 1992)

INTERNATIONAL SEARCH REPORT

information on patent family members

Inter xnal Application No
PCT/US 00/10567

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 5450098 A	12-09-1995	NONE	
US 5404176 A	04-04-1995	CA 2108851 A,C	11-03-1995
US 5596349 A	21-01-1997	JP 2760714 B	04-06-1998
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		JP 2804686 B	30-09-1998
		JP 6118920 A	28-04-1994
		JP 2846777 B	13-01-1999
		JP 6118921 A	28-04-1994
		JP 2846780 B	13-01-1999
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		JP 6138858 A	20-05-1994
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		JP 6161399 A	07-06-1994
		JP 3048771 B	05-06-2000
		JP 6165089 A	10-06-1994
		JP 6242754 A	02-09-1994
		US 5784040 A	21-07-1998
EP 573174 A	08-12-1993	AT 158435 T	15-10-1997
		DE 69313925 D	23-10-1997
		DE 69313925 T	29-01-1998
		JP 6051725 A	25-02-1994
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FR 2752633 A	27-02-1998	JP 8286634 A	01-11-1996
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		US 6069609 A	30-05-2000